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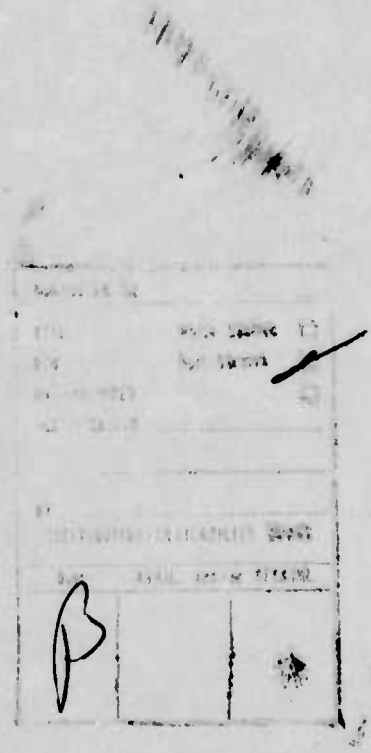
MDC E1125

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION - PHASE II

MOS/HYBRID STUDY

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

MCDONNELL DOUGLAS
CORPORATION



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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE II

9 AUG 1974

MDC-E1125

MOS/HYBRID STUDY

SUBMITTED TO:
CONTRACTING OFFICER
U.S. NAVAL WEAPONS LABORATORY
DAHLGREN, VA. 22448
CONTRACT NO. N00178-73-C-0362

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PREFACE

This document is one of eight task-oriented reports prepared under Contract No. N00178-73-C-0362 for the U. S. Naval Weapons Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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1. INTRODUCTION AND SUMMARY

Three major technology areas are available for device selection by military system designers: bipolar, MOS and hybrid. Devices fabricated by these different techniques may exhibit significant differences in the areas of RF susceptibility and eventual catastrophic failure.

This report documents a preliminary investigation into the possible differences between similar devices from the MOS and hybrid technology areas in comparison with previous data on bipolar devices. While it is difficult to compare the observed susceptibility and failure modes, it appears that the underlying RF susceptibility mechanism for devices from all three technology areas can be explained by rectification of the RF signal at the device pn junctions. The rectification site can be a normal device junction, as in hybrid and bipolar devices; a parasitic junction as in MOS, hybrid and bipolar devices; or a protective junction, as in most MOS devices. The circuit reaction to the rectified currents and voltages is different for all three types of devices but can be analyzed using normal circuit theory.

The mean power level required for the output voltage to cross the interference threshold level for the 7400 bipolar device, the 4011 CMOS device and the 2002 hybrid device falls within a 10 dB band at all four frequencies for the most susceptible port. The minimum power level required for catastrophic failure for all three devices also falls within a 10 dB band which is generally 30 dB above the minimum interference threshold band. It appears that these digital devices from the three major technology areas exhibit similar susceptibility characteristics and hence there appears to be no inherent advantage from this standpoint in using digital devices from any particular technology area.

2. RF SUSCEPTIBILITY MEASUREMENTS

As the complexity of military systems steadily increases, the usage of integrated circuits (ICs) and the various types of ICs used in these systems has also increased. System designers now have three major technology areas from which to choose their devices: bipolar, MOS and hybrid. Recent reports [1, 2, 3, 4, 5] have outlined the general RF susceptibility characteristics of both digital and linear bipolar devices. In light of these bipolar device results, it became highly desirable to determine whether a system designer could gain a significant improvement in overall system RF hardening by using devices fabricated by a technology other than bipolar. We are now examining this possibility by measuring the RF susceptibility characteristics of a digital CMOS device and a digital hybrid device and comparing their RF susceptibility characteristics with the previous digital bipolar device data.

2.1 MOS Interference Tests - MOS technology represents a growing segment of the integrated circuit arena as evidenced by a recent estimate forecasting that complementary MOS (CMOS) technology will surpass bipolar TTL technology in usage by 1976. The MOS technology can be roughly divided into three major areas: p-channel, n-channel and complementary (a combination of both p-channel and n-channel). There are many MOS subtechnologies: silicon gate, metal gate, dielectric isolated, silicon-on-sapphire, etc. The CMOS devices are particularly attractive for study because both p-channel and n-channel MOS transistors are fabricated on the same chip. Most CMOS devices utilize a metal gate process but for very low supply voltages (1 volt), a silicon gate process is used. The CMOS technology can also be used to manufacture both digital and linear devices on the same chip (performing some functions previously relegated only to hybrid ICs.)

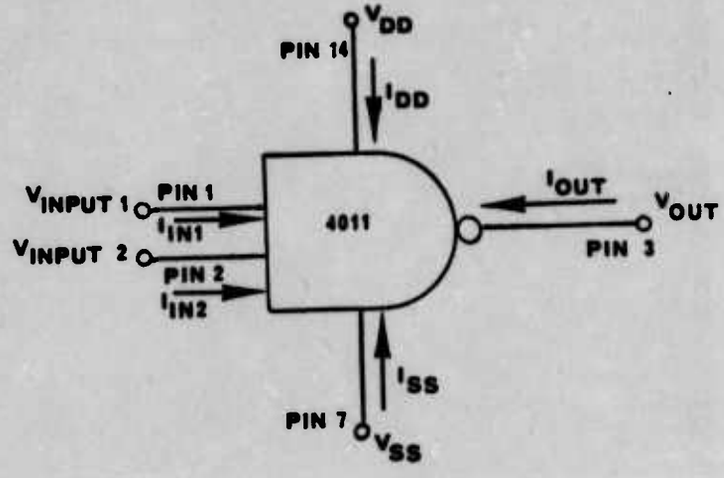
In addition, CMOS devices possess many advantageous characteristics which have led to their ever-increasing utilization in complex military electronic systems: a very high DC input impedance (typically 10^{12} ohm with picofarads of capacitance),

very low quiescent power drain (typically nanowatts), high noise immunity (typically 30% of power supply, V_{DD}) and the capability of operating from a power supply over the range of 3 to 15 volts. For these reasons and for ease of comparison with the bipolar 7400 NAND gate, a CMOS 4011 NAND gate was chosen for study.

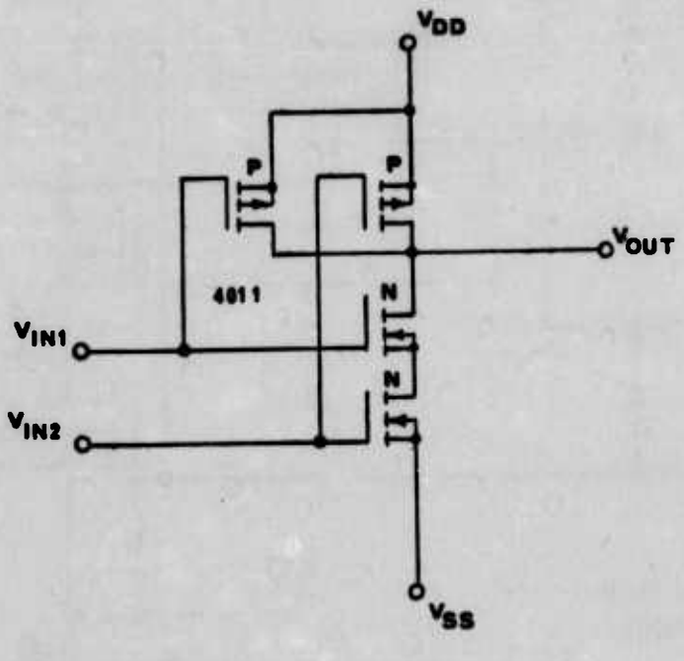
2.1.1 CMOS NAND Gate - The 4011 is a CMOS quad 2-input NAND gate having the same schematic representation as the bipolar 7400 NAND gate, although they are not pin-for-pin or function-for-function interchangeable. The circuit diagram for the 4011 NAND gate is shown in figure 1 with the current and voltage conventions used in this report. A photomicrograph of a two-input NAND gate (the one gate of the four on the 4011 chip which was used for all RF testing) is shown in figure 2.

Most CMOS devices require some type of protective circuitry for all gate inputs accessible to the outside world. The protective circuitry for the 4011 NAND gate used in this RF testing is shown in figure 3. Also shown in figure 3 are the parasitic junctions formed during fabrication of the 4011. An illustration of how these parasitic junctions are formed during device fabrication is shown in figure 4. Even with the protective circuitry, proper care of these devices is essential. The protective circuitry has no noticeable effect on circuit speed and does not interfere with normal device operation.

2.1.2 4011 Test Circuit - The dc bias circuitry used for RF susceptibility testing of the 4011 device is shown in figure 5. The input loading was chosen to simulate a nominal CMOS-CMOS interface while the output loading was chosen for the maximum source and sink current specified, a worst case output interface condition. The schematic diagram for the 4011 interference measurement system is shown in figure 6. This system measures the dc parameters of voltage and current at each of the five ports for the NAND gate tested and also measures the RF parameters of incident power, reflected power, and absorbed power. The measurement system is discussed in the Test and Measurement System Report [6].



4011 SCHEMATIC DIAGRAM



4011 CIRCUIT DIAGRAM

FIGURE 1 4011 SCHEMATIC AND CIRCUIT DIAGRAM

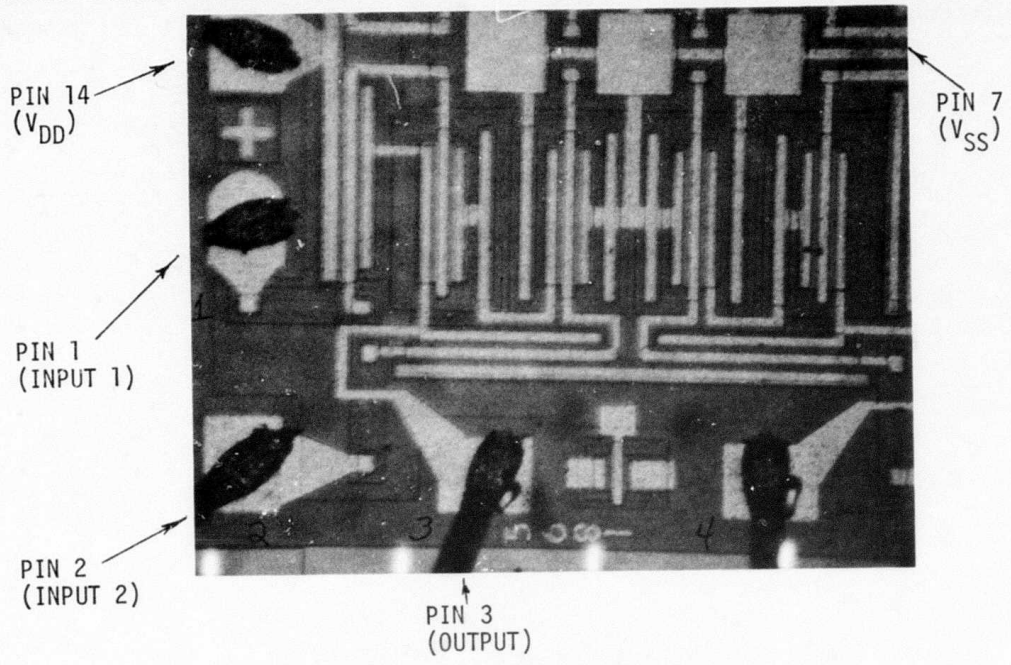


FIGURE 2 PHOTOMICROGRAPH OF CMOS 4011 NAND GATE

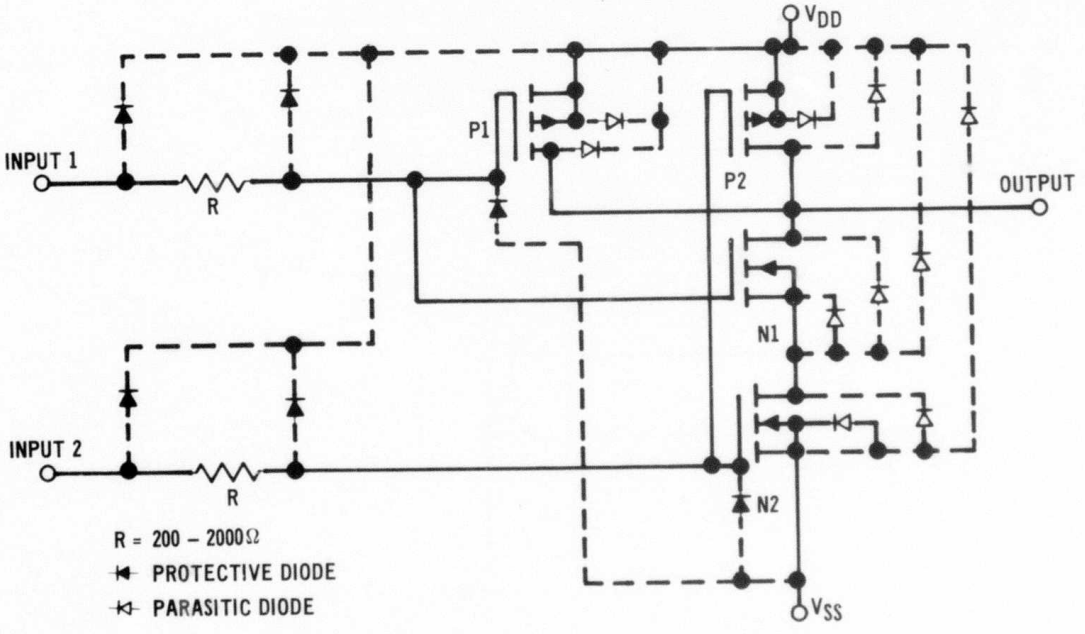


FIGURE 3 4011 CIRCUIT DIAGRAM SHOWING ALL PN JUNCTIONS
(Parasitic and Protective Junctions Indicated by Dashed Lines)

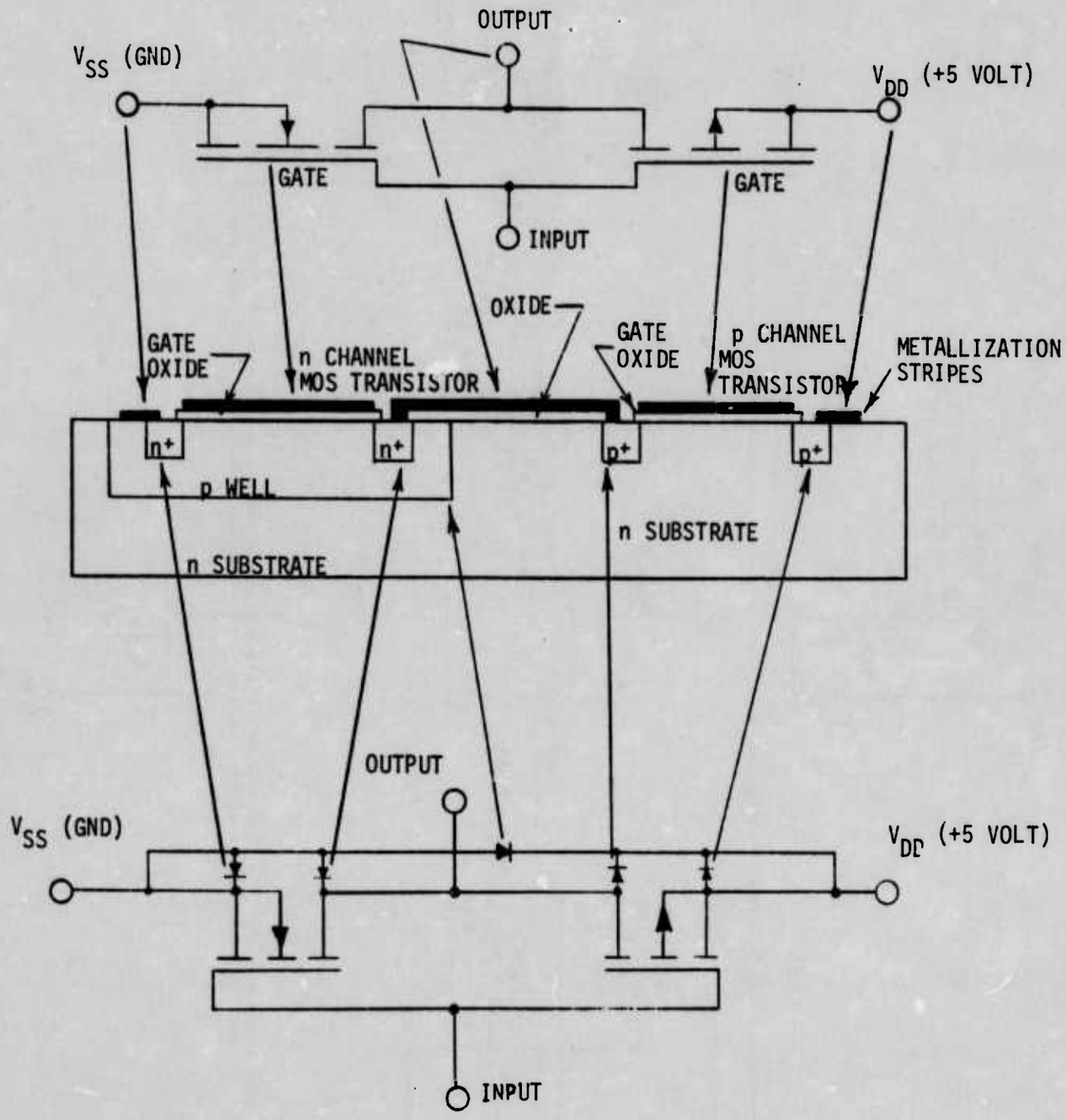


FIGURE 4 CROSS-SECTION OF TYPICAL CMOS DEVICE SHOWING THE PARASITIC JUNCTIONS AND THEIR SCHEMATIC REPRESENTATION

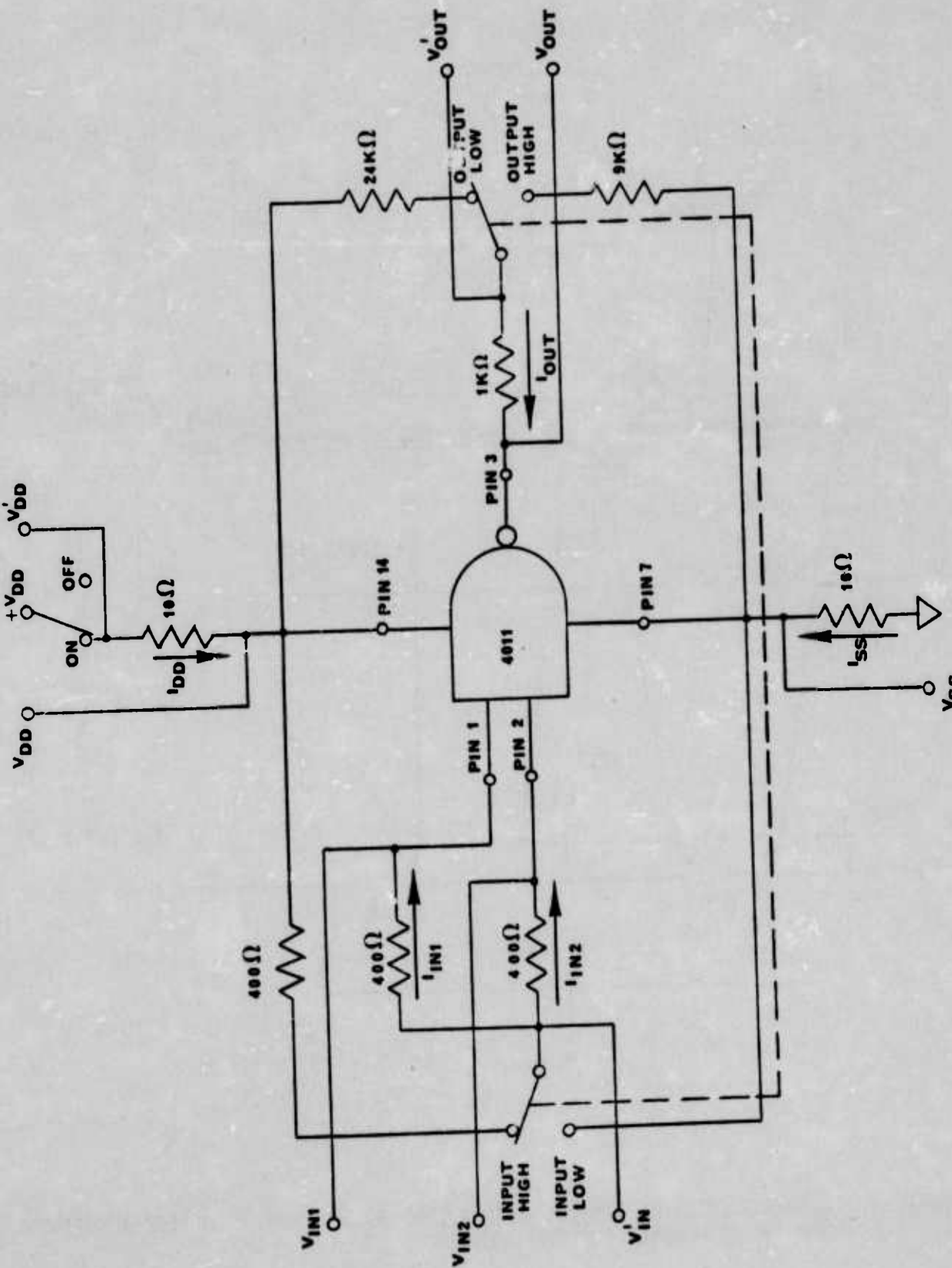


FIGURE 5 4011 BIAS CIRCUITRY

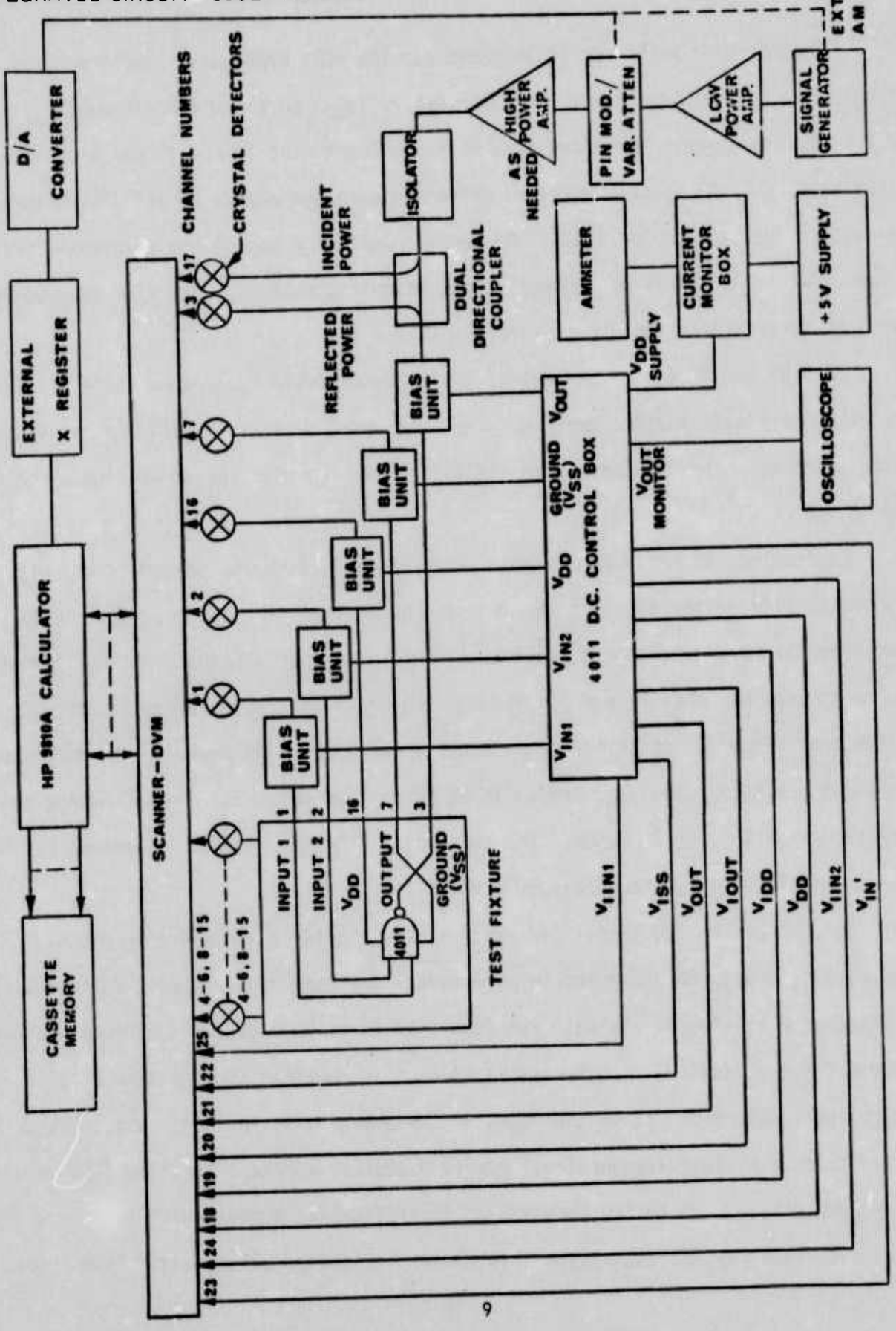


FIGURE 6 4011 AUTOMATED MEASUREMENT SYSTEM SCHEMATIC

Five RF entry ports are of interest for the 4011 NAND gate: two identical input ports, the output port, the power supply (V_{DD}) port and the ground (V_{SS}) port. Since the input ports are identical, only one input port (input 2) was used for RF injection. All RF measurements are performed with the output of the 4011 DC-biased in either the high or low state. No dynamic switching conditions were considered other than the possible RF induced output state transitions. The flow diagram for 4011 RF interference testing is shown in figure 7.

Both RF and DC device parameters are measured while subjecting the 4011 device to RF power levels ranging from maximum RF (power capability of measurement system) down to no RF. The RF effects can easily be compared with the no RF case using this technique.

Exploratory RF measurements were performed at 910 MHz to determine the relative susceptibility of the 4011 with RF incident on the various device ports. These measurements were used as a guide for all future 4011 RF testing. The 4011 proved to be susceptible when RF was incident on the input and output ports (an output state transition was noted for these cases under maximum RF power). The other two RF input ports, V_{DD} and V_{SS}, proved to be not susceptible with minimal output state variations at maximum RF power. For this reason the susceptibility testing of the unsusceptible ports was not pursued further.

Because of the additional information required for this device in another report [7], twenty RF power levels were chosen for each device configuration tested. Interference testing of the 4011 was specified to include the 20 different RF power levels for each device, with 5 devices at each susceptible RF injection port (previously determined to be the input and output ports), for each output logic state at each of four frequencies. Figure 8 depicts a data processing flow diagram for these data. Each device receives an identification number which is entered into the measurement system manually. This number identifies all cassette tape files.

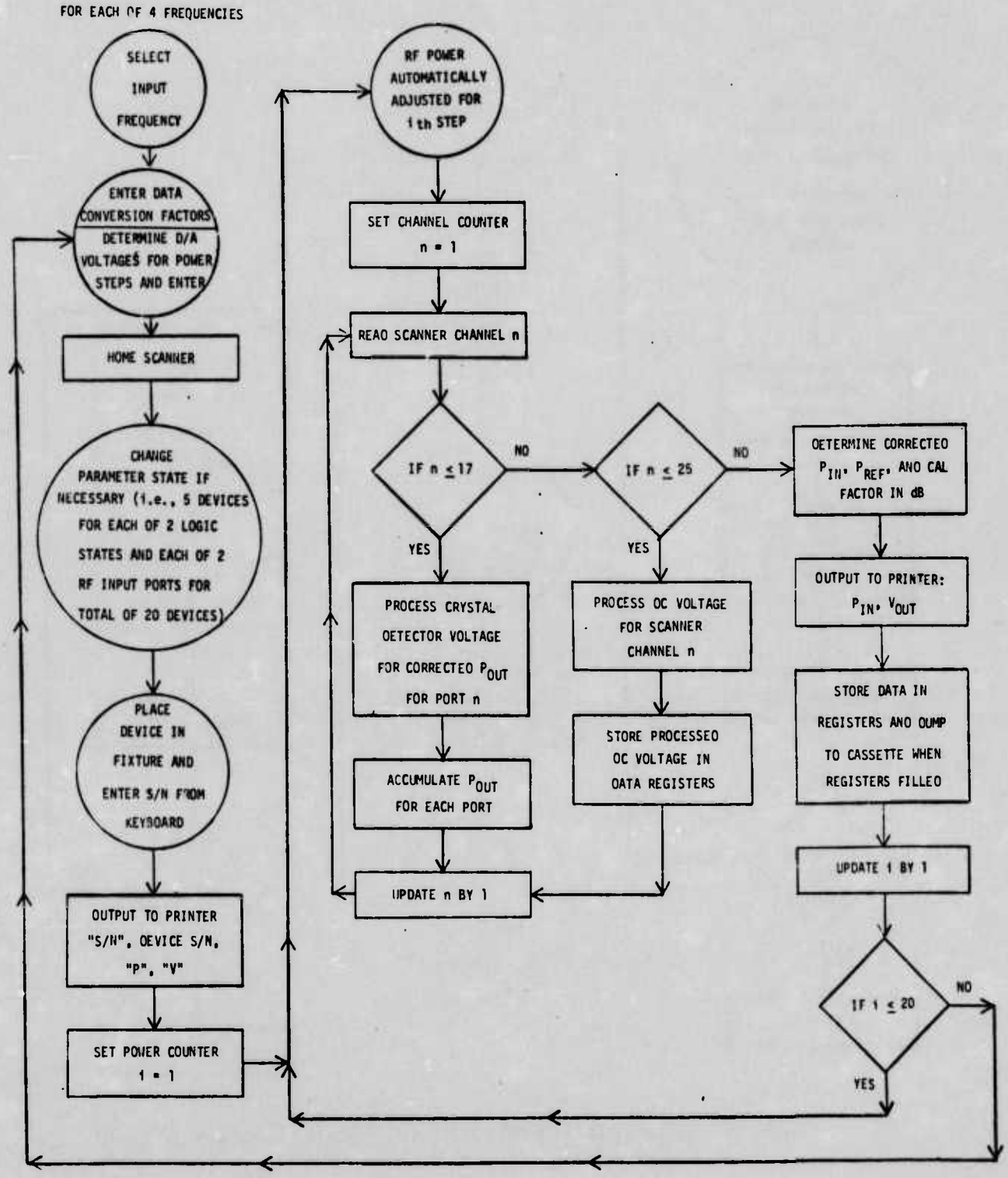


FIGURE 7 4011 INTERFERENCE TEST FLOW DIAGRAM

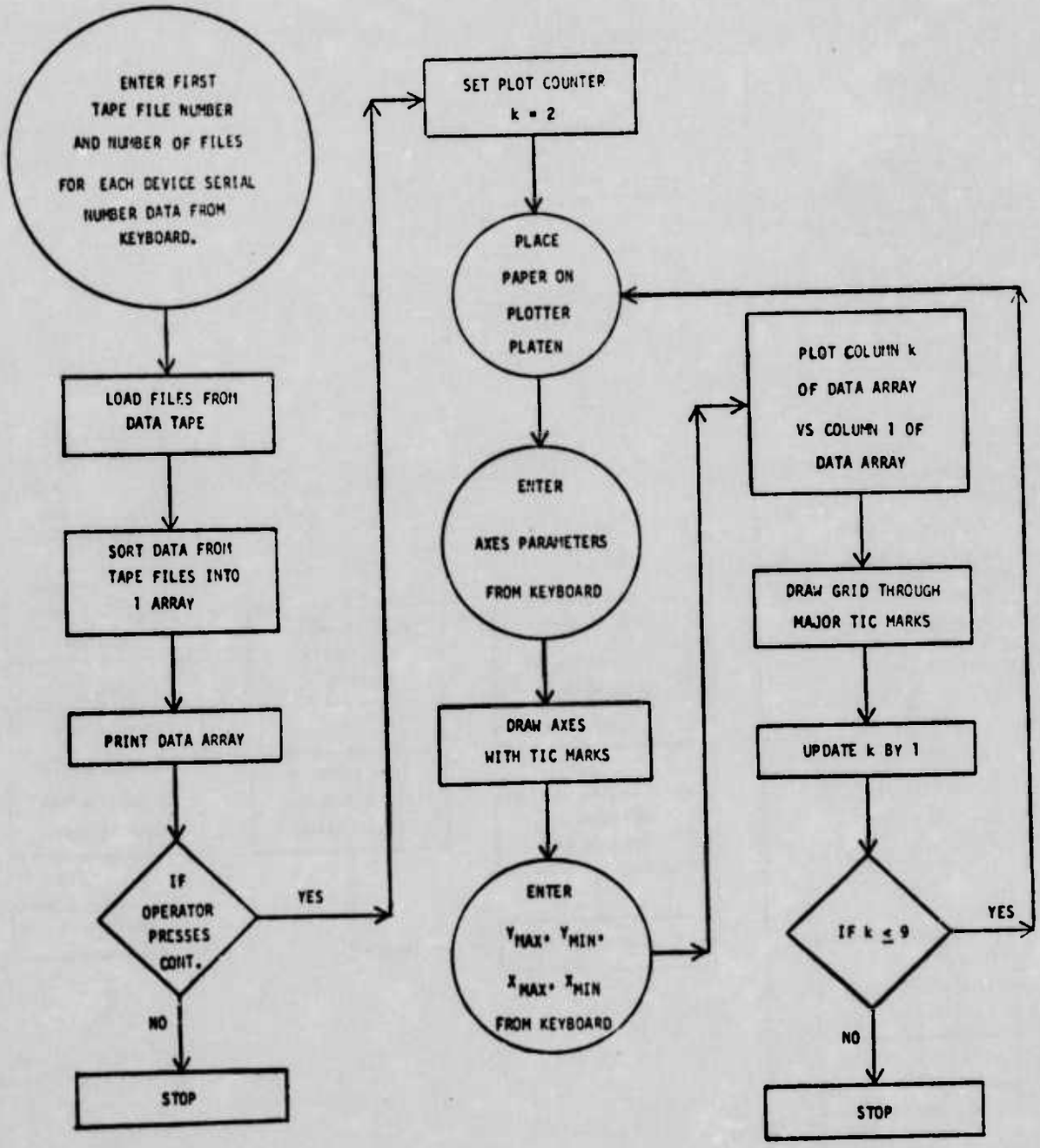


FIGURE 8 4011 INTERFERENCE TEST DATA REDUCTION FLOW DIAGRAM

All data processing routines, printouts and plots are generated from these cassette tapes on an HP 9830A computer. A typical data matrix printout is shown in Table 1.

2.1.3 4011 Interference Test Results - RF interference data on the 4011 were taken at four frequencies for the injection ports previously found to be susceptible. Data plots of these 4011 output voltage variations due to RF power are shown in figures 9 and 10 for RF injected into the input port with the output high and the output low respectively. Data plots of 4011 output voltage variations due to RF power are shown in figures 11 and 12 for RF injected into the output port with the output high and the output low respectively. It can be seen that the 4011 has two susceptible configurations: RF injected into the input port with the output low and and RF injected into the output port with the output low. The RF effects tend to diminish with increasing frequency as in the case of the bipolar 7400 NAND gate. As outlined in the MOS NAND Gate Study [7], the susceptibility threshold of the 4011 and the 7400 NAND gates are very similar for their most susceptible configuration and the primary RF effects in both devices can be explained by rectification of the RF signal at the device pn junctions.

2.2 Hybrid Interference Tests - The hybrid technology is normally used where the required device function to be performed involves using components that cannot be efficiently fabricated on a single chip. The hybrid circuit is normally built up from separate chips bonded on a common substrate, jumpered accordingly and enclosed in a single IC package. Most common bipolar and MOS devices (gates, etc.) are never manufactured using the hybrid technology because it is not practical or economical. Therefore a readily available, representative hybrid device utilizing NAND logic was selected for RF testing: the 2002 DTL High Power Driver.

2.2.1 Hybrid High Power Driver - The 2002 consists of three chips: two DTL quad input NAND gates on one chip, a diffused nichrome resistor on another chip and the high power output transistor on another chip. A photomicrograph of these chips on

Table 1 TYPICAL 4011 DATA PRINTOUT

S/N= 1203

Pd(mW)	Pr(mW)	CF(dB)	Vdd	Idd	Iout	Vout	Iss	Iinrf	Vinrf	Vin1
-0.000	0.000	0.00	4.988	0.300	0.194	0.150	-0.19	0.010	4.976	4.976
0.007	1.673	24.06	4.988	0.300	0.194	0.151	-0.19	0.045	4.949	4.963
0.091	1.828	13.68	4.988	0.300	0.194	0.151	-0.19	0.050	4.943	4.960
0.268	2.074	9.86	4.988	0.300	0.194	0.152	-0.19	0.065	4.932	4.954
0.413	2.244	8.55	4.988	0.300	0.194	0.152	-0.19	0.078	4.923	4.950
0.719	2.531	7.05	4.988	0.300	0.194	0.152	-0.19	0.095	4.908	4.942
1.291	2.949	5.70	4.988	0.300	0.194	0.153	-0.19	0.125	4.883	4.930
2.371	3.547	4.55	4.988	0.300	0.194	0.154	-0.19	0.178	4.842	4.910
3.988	4.247	3.78	4.988	0.200	0.194	0.156	-0.19	0.243	4.790	4.883
6.260	5.079	3.25	4.988	0.300	0.194	0.158	-0.19	0.325	4.725	4.851
10.010	6.276	2.84	4.988	0.200	0.194	0.161	-0.19	0.443	4.631	4.804
17.000	8.739	2.64	4.988	0.300	0.193	0.168	-0.19	0.665	4.451	4.713
26.759	11.047	2.35	4.988	0.200	0.193	0.177	-0.20	0.868	4.288	4.632
47.871	16.930	2.22	4.988	0.200	0.191	0.223	-0.22	1.310	3.936	4.456
72.187	23.325	2.16	4.987	0.300	0.189	0.308	-0.28	1.693	3.630	4.304
114.368	33.559	2.11	4.986	0.400	0.179	0.549	-0.39	2.228	3.197	4.089
180.791	50.455	2.11	4.984	0.600	0.141	1.333	-0.59	2.960	2.614	3.795
266.745	68.819	2.07	4.984	0.600	0.105	2.505	-0.60	3.543	2.140	3.557
419.195	96.626	1.99	4.965	0.500	0.072	3.068	-0.50	4.280	1.557	3.266
655.173	116.647	1.79	4.985	0.500	0.110	3.006	-0.46	4.750	1.189	3.075

P_d = POWER DISSIPATED IN CHIP

P_r = POWER REFLECTED FROM CHIP

ALL VOLTAGES IN VOLTS

ALL CURRENTS IN MILLIAMPS

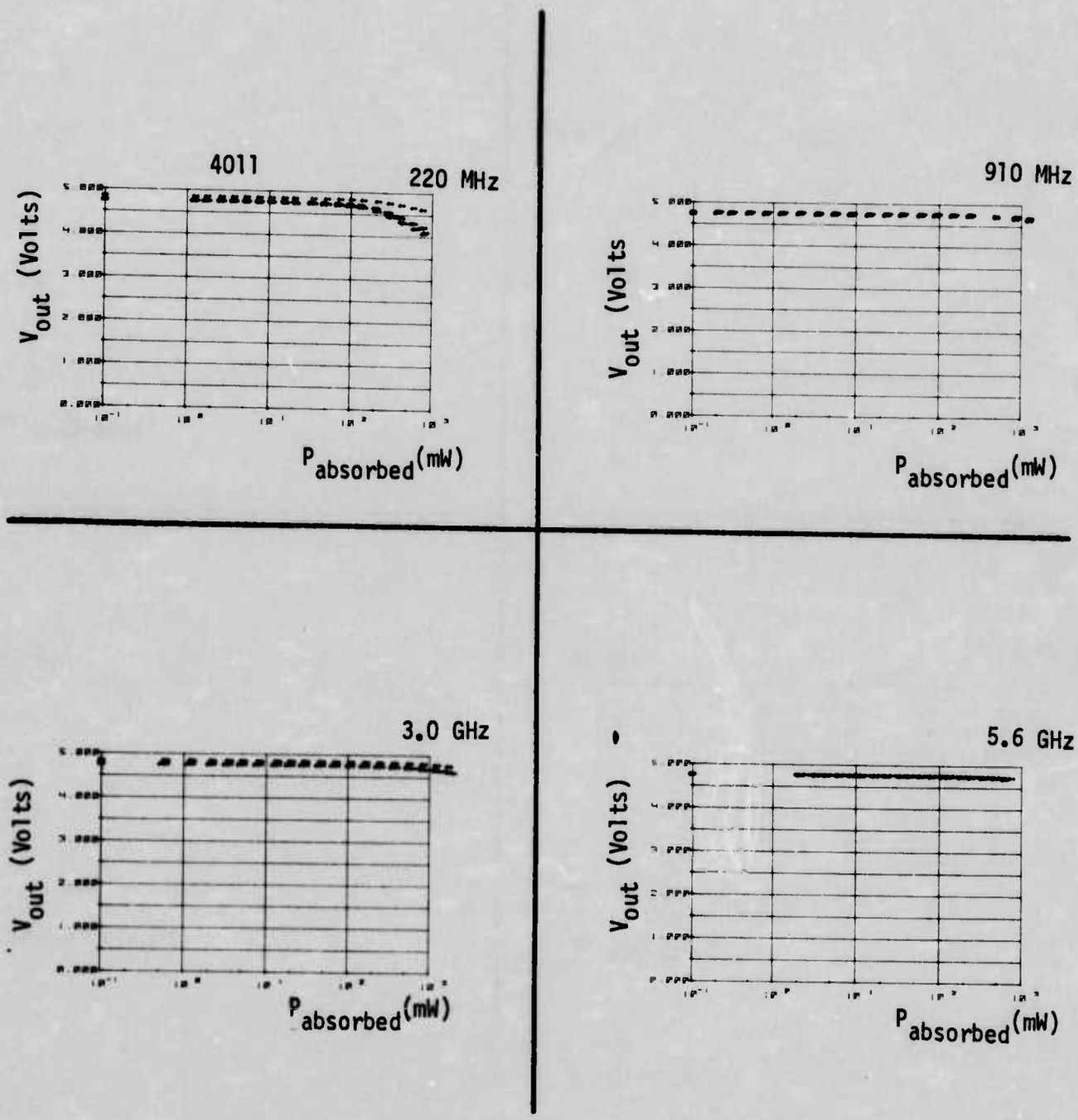


FIGURE 9 4011 INTERFERENCE DATA FOR RF INJECTED INTO THE INPUT PORT WITH THE OUTPUT HIGH

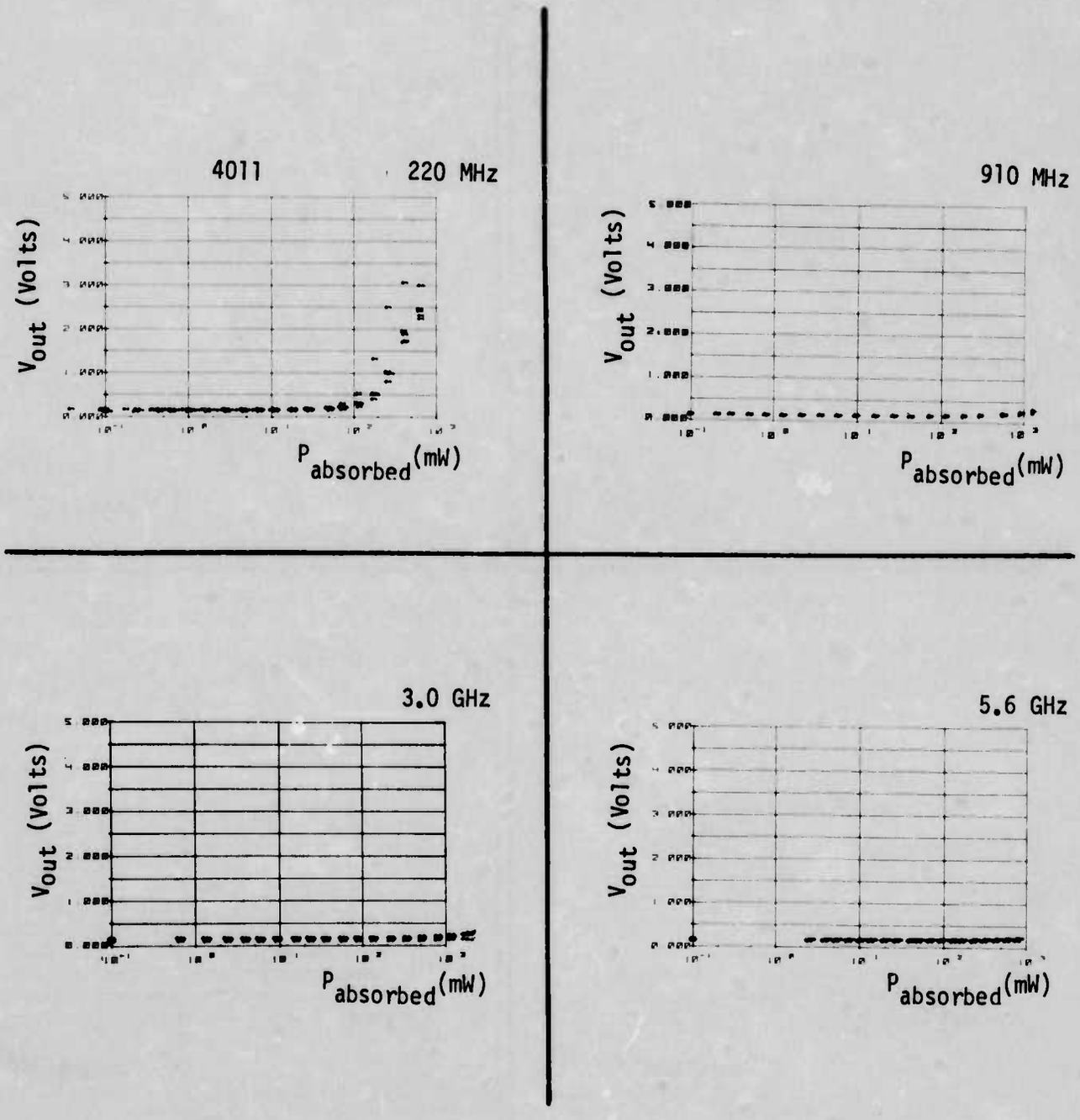


FIGURE 10 4011 INTERFERENCE DATA FOR RF INJECTED INTO THE INPUT PORT WITH THE OUTPUT LOW

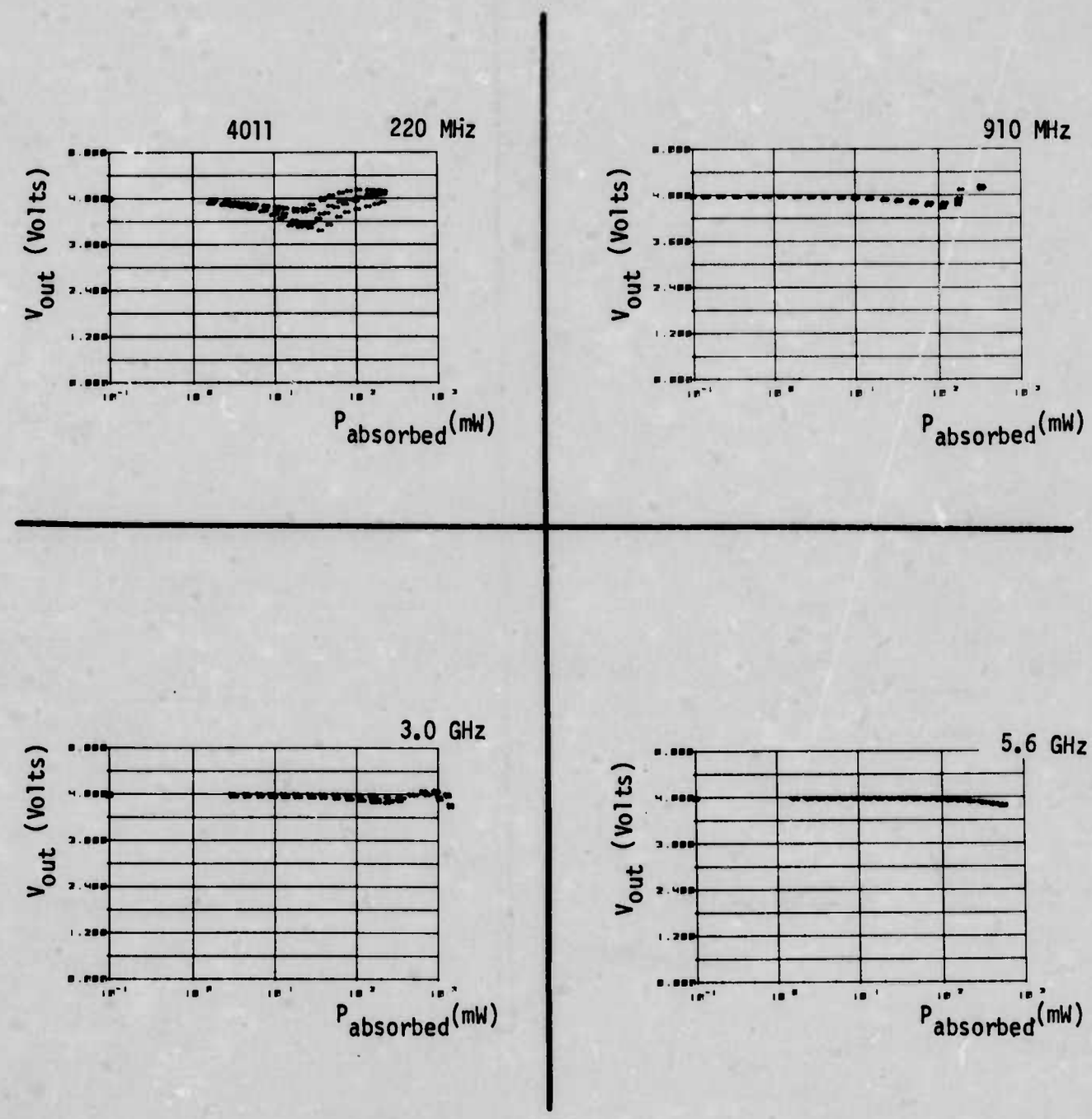


FIGURE 11 4011 INTERFERENCE DATA FOR RF INJECTED INTO THE OUTPUT PORT WITH THE OUTPUT HIGH

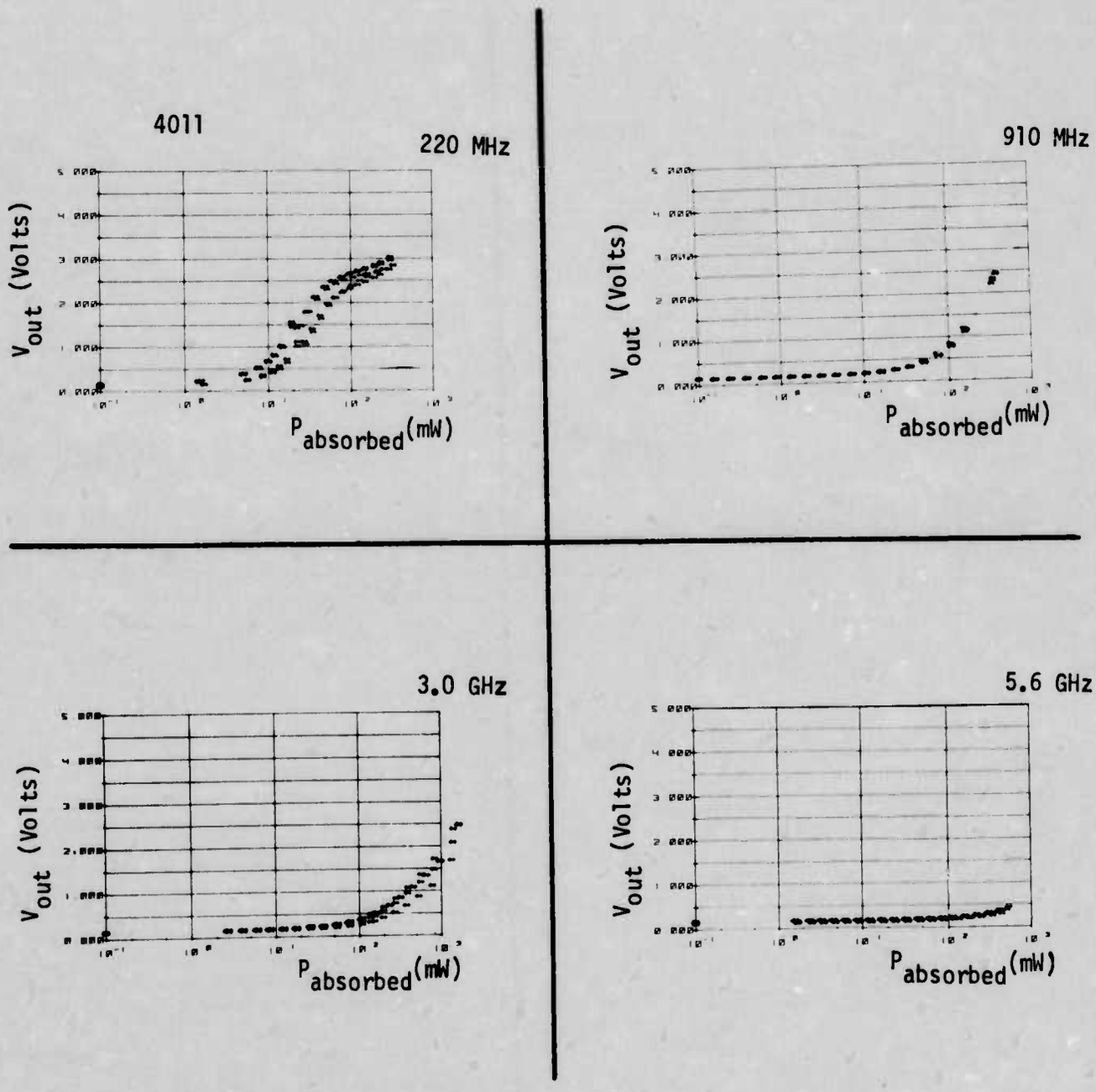


FIGURE 12 4011 INTERFERENCE DATA FOR RF INJECTED INTO THE OUTPUT PORT WITH THE OUTPUT LOW

the common substrate is shown in figure 13 along with its schematic representation. The circuit diagram of the 2002 is shown in figure 14. Although the schematic representation of the 2002 hybrid device is similar to the bipolar 7400 NAND gate (TTL), the 2002 logic is DTL. This is the first bipolar DTL device to be included in the RF susceptibility investigation.

2.2.2 2002 Test Circuit - The 2002 High Power Driver may be used in many different circuit applications. For ease of testing and to minimize instrumentation problems, the bias circuit of figure 15 was chosen for the 2002. The DTL NAND gate input loading simulates a typical TTL output (a TTL-DTL interface). The loading of the output transistor of the 2002 simulates a high current ($\tilde{\approx}$100 mA) load at 5 volts, a typical lamp or relay driver application.

The automated measurement system used for 2002 interference testing is discussed in the Test and Measurement Systems Report [6]. The schematic diagram for the 2002 interference measurement system is shown in figure 16.

There are ten possible RF entry ports into the 2002 device. The logic circuitry of the 2002 consists of two identical NAND gates in series. Since all the diode coupled inputs are identical, a representative input port was chosen for RF injection: pin 9. The other possible RF input ports are the power supply and ground ports, the base (through a resistor) of the output transistor, and the emitter and collector of the output transistor. All RF measurements were performed with the 2002 DC-biased with the output transistor either on or off. No dynamic switching conditions were considered except those due to RF effects.

The 2002 RF interference test flow diagram is very similar to the 4011 RF interference test flow diagram of figure 7. The 2002 device parameters were measured for two automated runs at four RF power levels per run, similar to the RF interference testing of the susceptibility survey devices [8]. The eight RF power levels used for RF injection ranged from no RF (a DC parameter run) to maximum RF

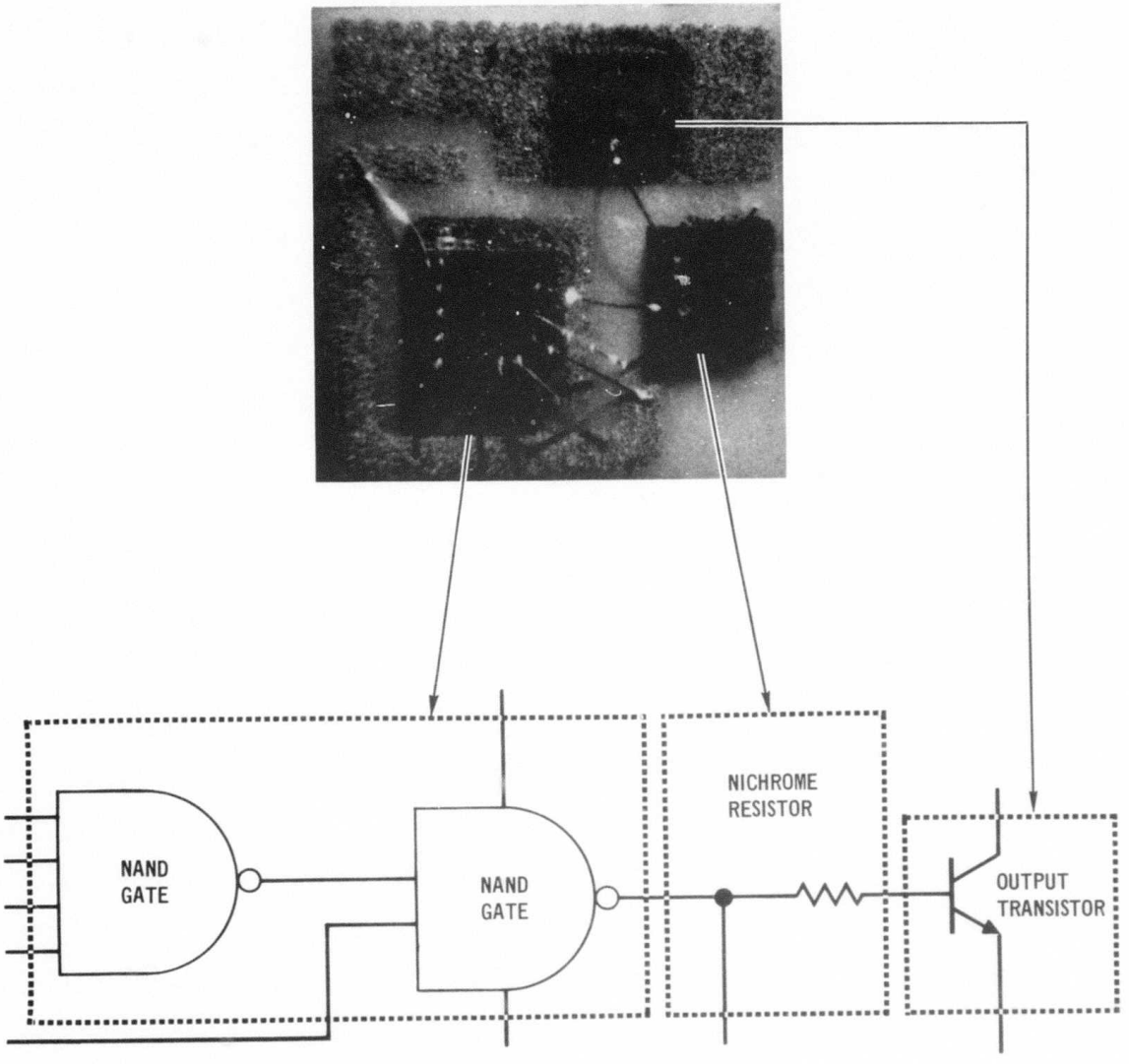


FIGURE 13 2002 CHIP LAYOUT & FUNCTIONAL SCHEMATIC

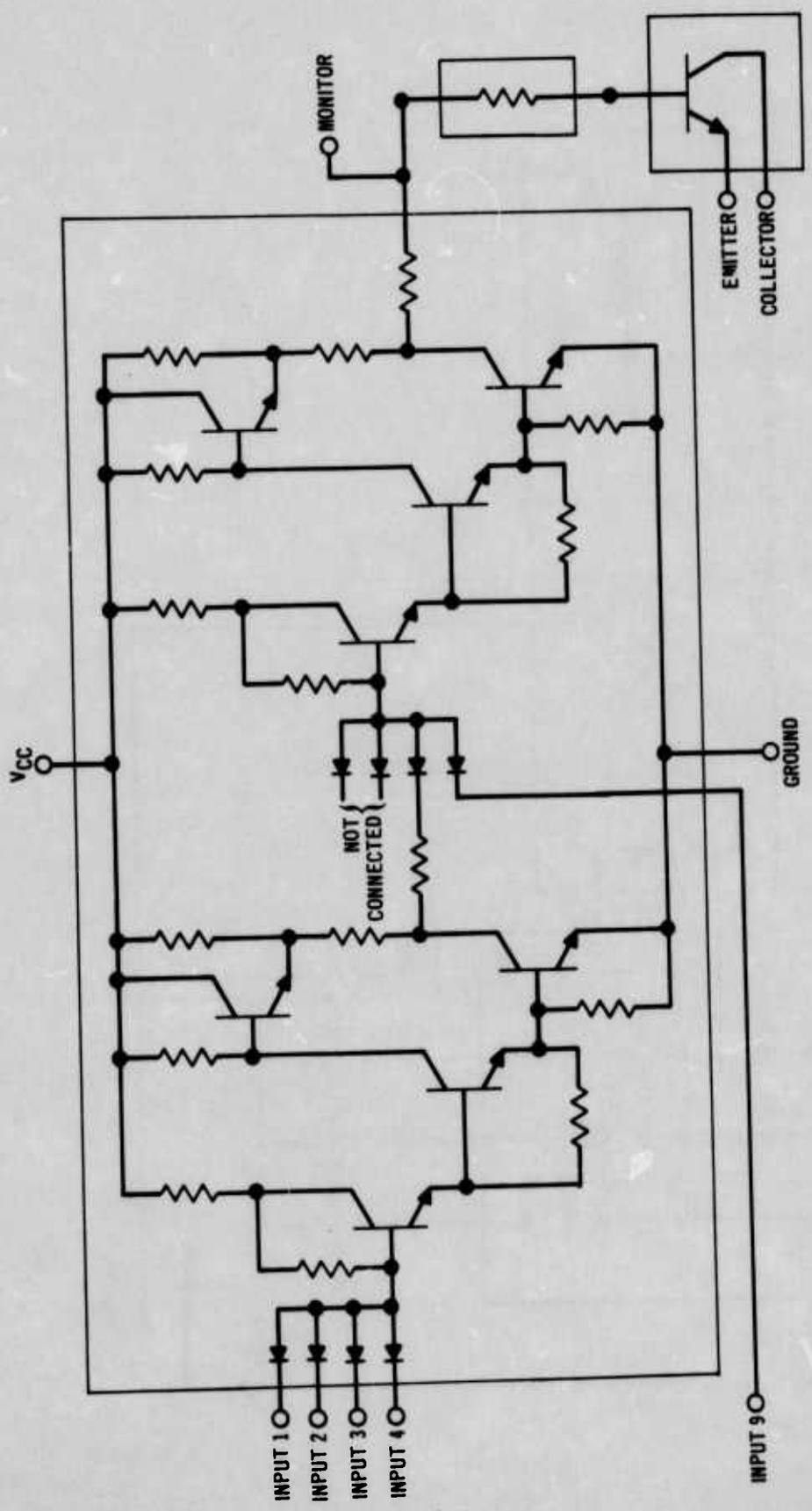


FIGURE 14 2002 CIRCUIT DIAGRAM

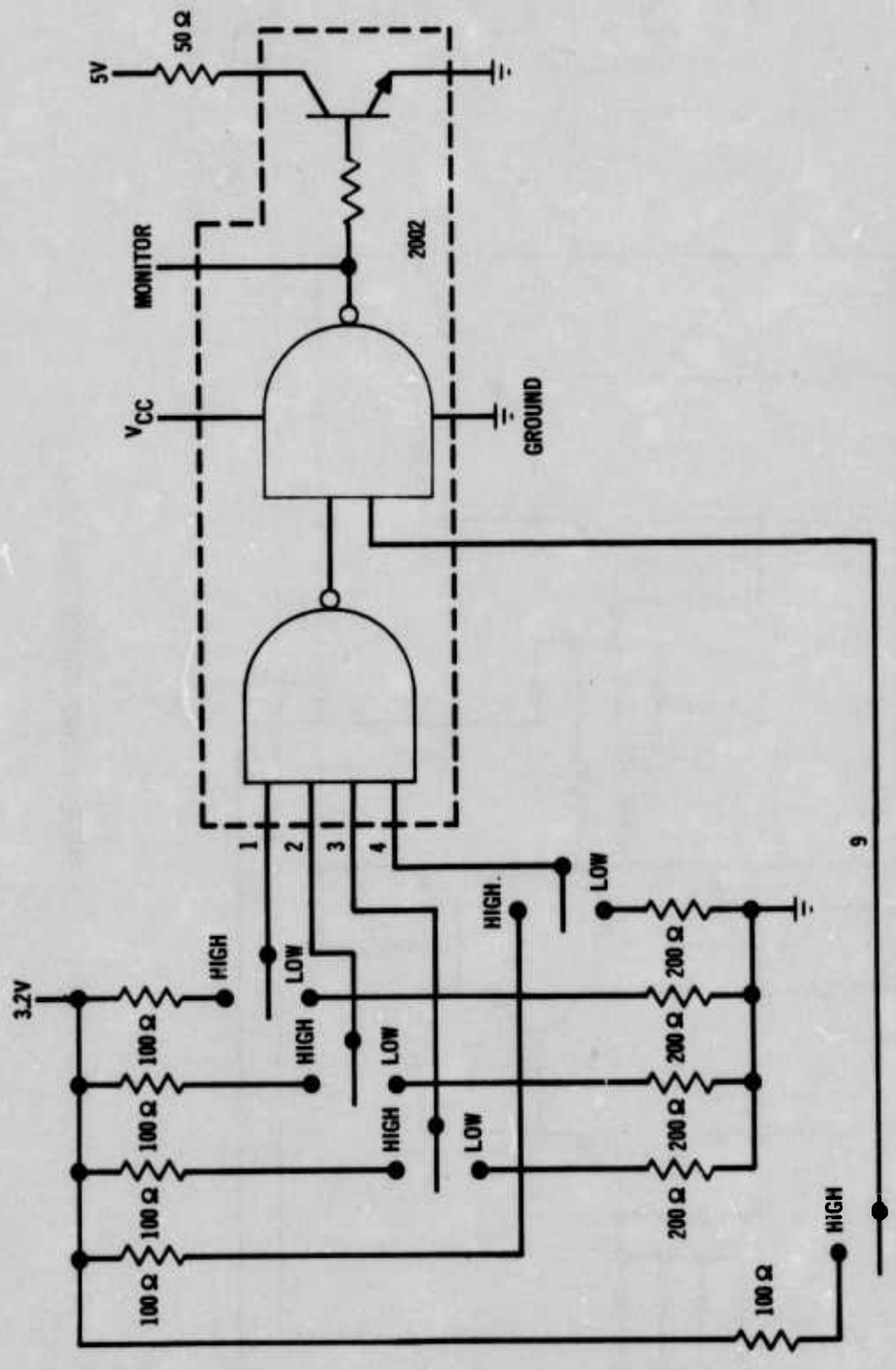


FIGURE 15 BIAS CIRCUIT FOR 2002

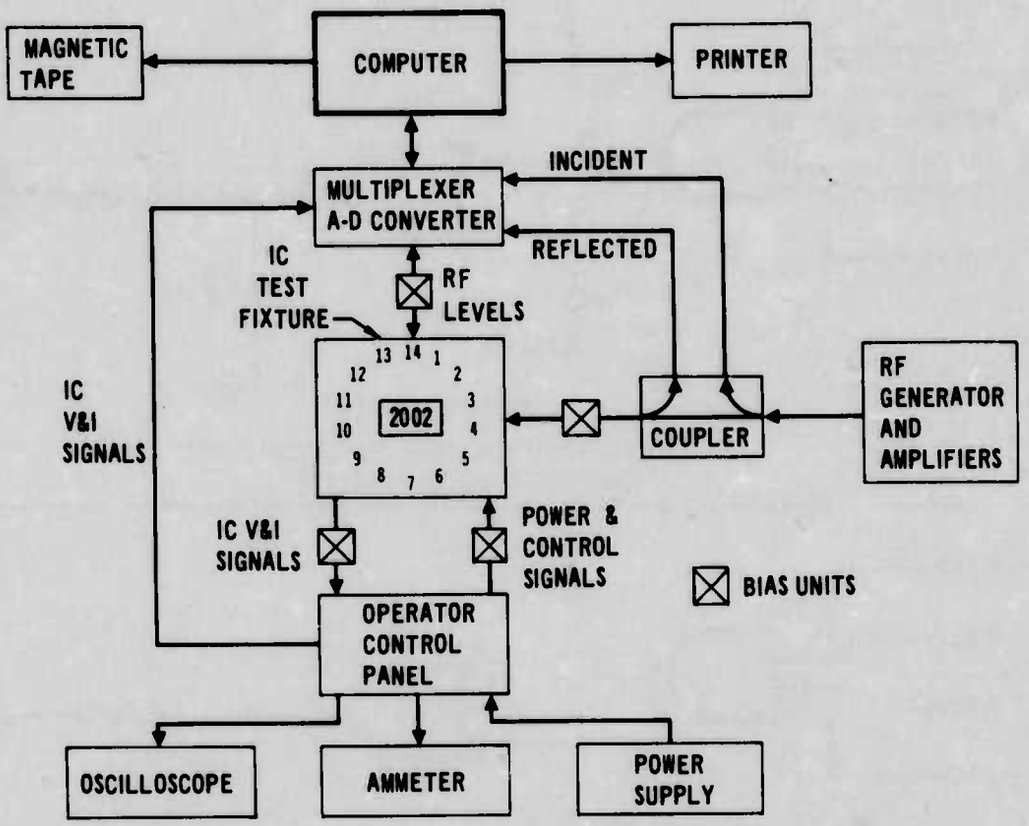
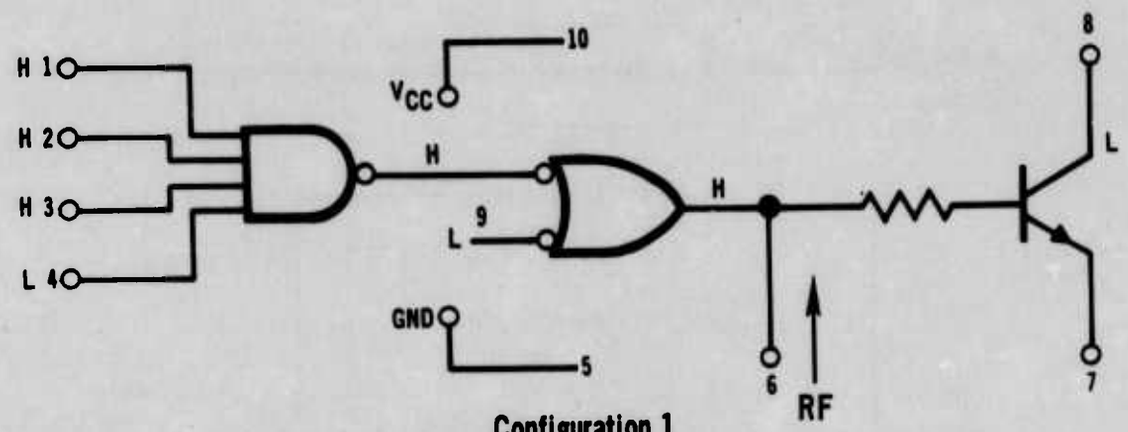


FIGURE 16 SCHEMATIC DIAGRAM FOR 2002 AUTOMATED MEASUREMENT SYSTEM

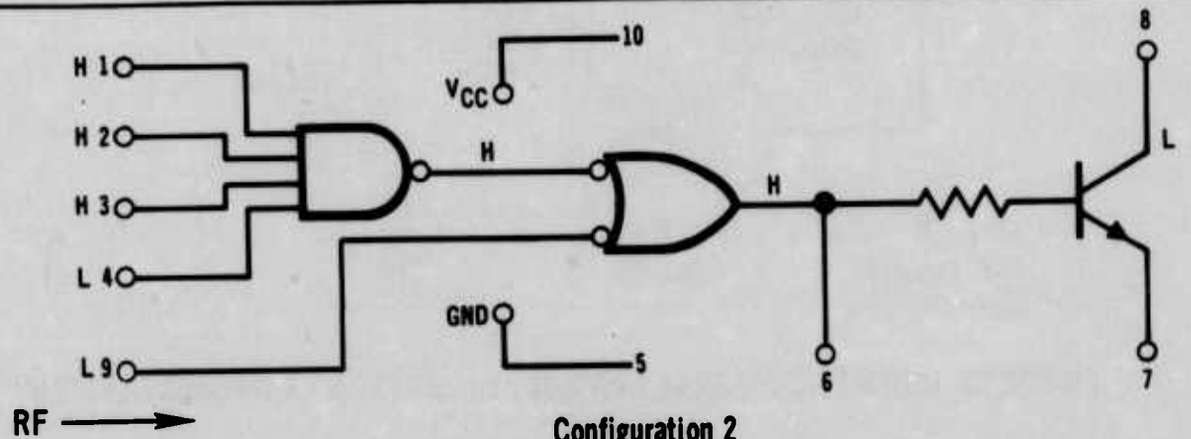
power. The RF power levels were chosen to convey the maximum information for each discrete RF power level.

Exploratory RF susceptibility measurements were performed on the 2002 at 220 MHz to determine the susceptibility of the aforementioned 2002 ports: pin 5 (ground port), pin 6 (NAND gate logic output and base of output transistor through a resistor), pin 7 (emitter of output transistor), pin 8 (collector of output transistor), pin 9 (NAND gate logic input), and pin 10 (power supply). Several logic state configurations were used for the various RF injection ports. This testing indicated that three 2002 configurations were susceptible to RF power at 220 MHz. The susceptibility testing was then limited to the three test configurations shown in figure 17.



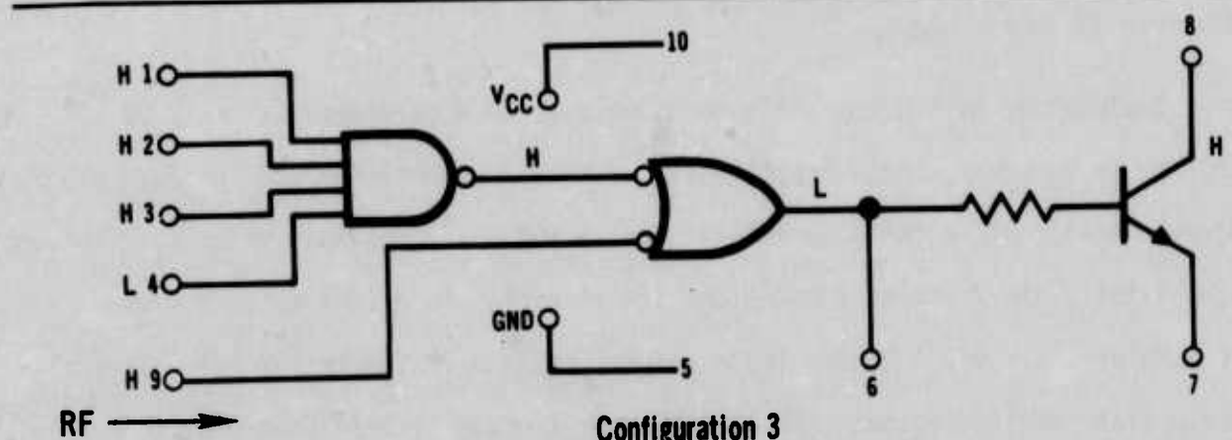
Configuration 1

RF INJECTED INTO NAND GATE LOGIC OUTPUT PORT,
NAND GATE LOGIC OUTPUT STATE HIGH



Configuration 2

RF INJECTED INTO NAND GATE INPUT PORT,
NAND GATE LOGIC OUTPUT STATE HIGH



Configuration 3

RF INJECTED INTO NAND GATE INPUT PORT,
NAND GATE LOGIC OUTPUT STATE LOW

H – HIGH STATE
L – LOW STATE

FIGURE 17 THREE 2002 CIRCUIT CONFIGURATIONS FOR RF SUSCEPTIBILITY TESTING

For each of the three susceptible 2002 test configurations, RF interference testing was completed for five devices at each of four frequencies. An identification number is given to each device and this number is recorded on the cassette tape along with the data. This number identifies all cassette tape files, data printouts, data plots, etc., associated with a given device. The data processing techniques are very similar to those shown previously for the 4011 data.

2.2.3 2002 Interference Test Results - RF interference data on the 2002 hybrid devices are plotted in figures 18, 19, and 20. These data depict the 2002 output transistor characteristics for the three susceptible configurations at the four test frequencies. The RF effects tend to diminish with increasing frequency as in the case of the bipolar NAND gate and the susceptibility thresholds are very sharply defined for individual devices.

The 2002 test results in figure 18 (configuration 1) demonstrate a susceptibility that has not previously been apparent in most data on 7400 and 4011 devices: an output transistor state transition from low to high with RF injected into the NAND gate output. This output transistor transition corresponds to a NAND gate output logic state transition from high to a low state. The RF input port for the 2002 in this case is the NAND gate output which is also the base of the output transistor after going through the nichrome resistor. For this RF input port it is difficult to determine the path of the RF although it appears to be affecting the output logic circuitry of the NAND gate. The 2002 is susceptible for this configuration at only 220 MHz and for only two of the five devices tested. At 220 MHz the susceptibility threshold for the two susceptible devices is very near the maximum power capability of the test system which probably causes the apparent erratic susceptibility.

The 2002 test results in figure 19 (configuration 2) are very similar to the corresponding 7400 test results. The susceptibility threshold at 220 MHz is

approximately 200 mW (absorbed power level in device) and increases gradually with increasing frequency.

The 2002 test results in figure 20 (configuration 3) demonstrated a susceptibility window where the device is susceptible for a given range of power levels and is unsusceptible both above and below this power level range. At 220 MHz this susceptibility window begins at an absorbed power level of ≈7 mW and ends at ≈50 mW. At 910 MHz the window is shifted to a slightly higher power level and at 3.0 GHz and 5.6 GHz the susceptibility disappears. This configuration is the most susceptible 2002 case at 220 and 910 MHz.

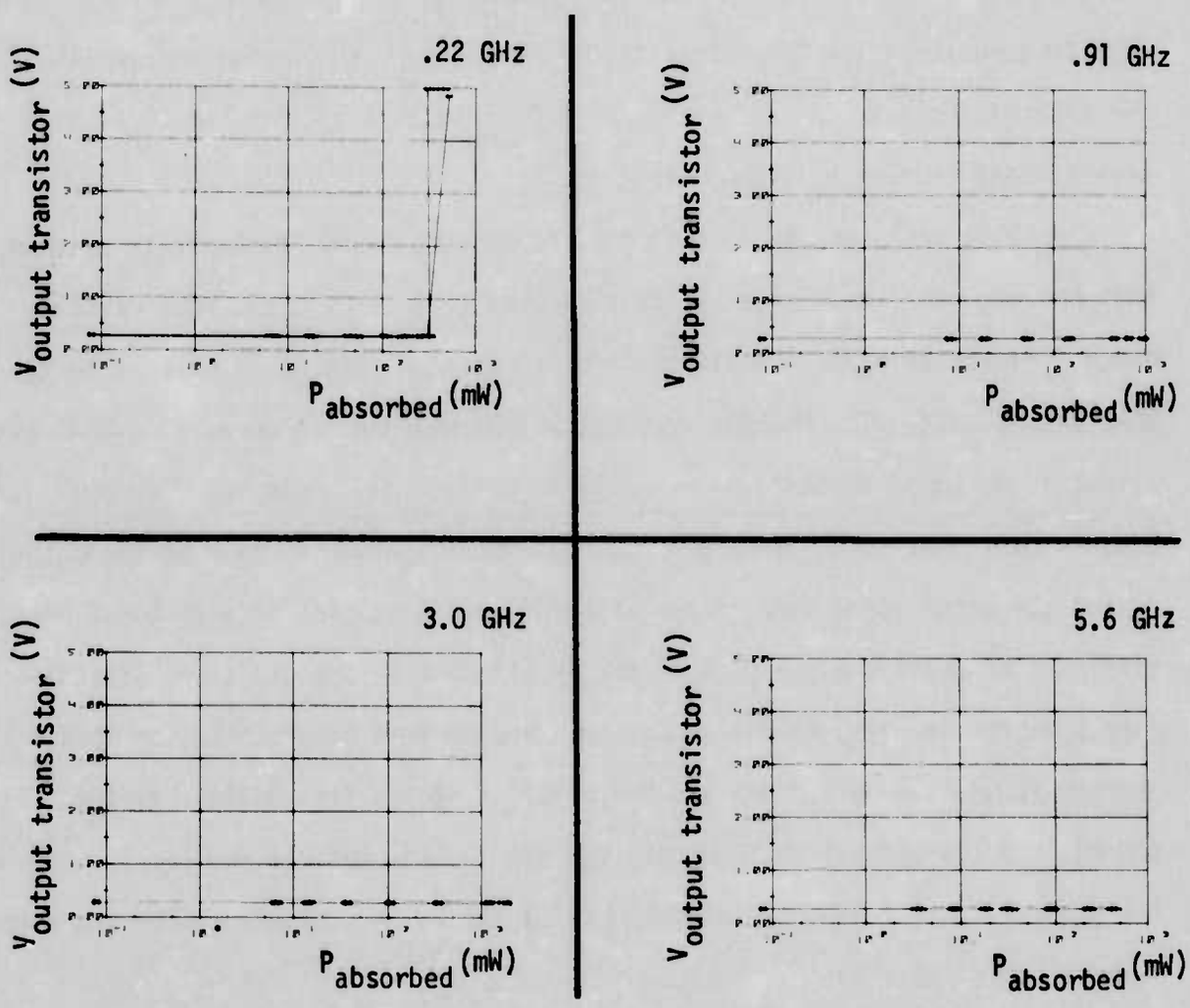


FIGURE 18 2002 INTERFERENCE DATA FOR RF INJECTED INTO THE NAND GATE OUTPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

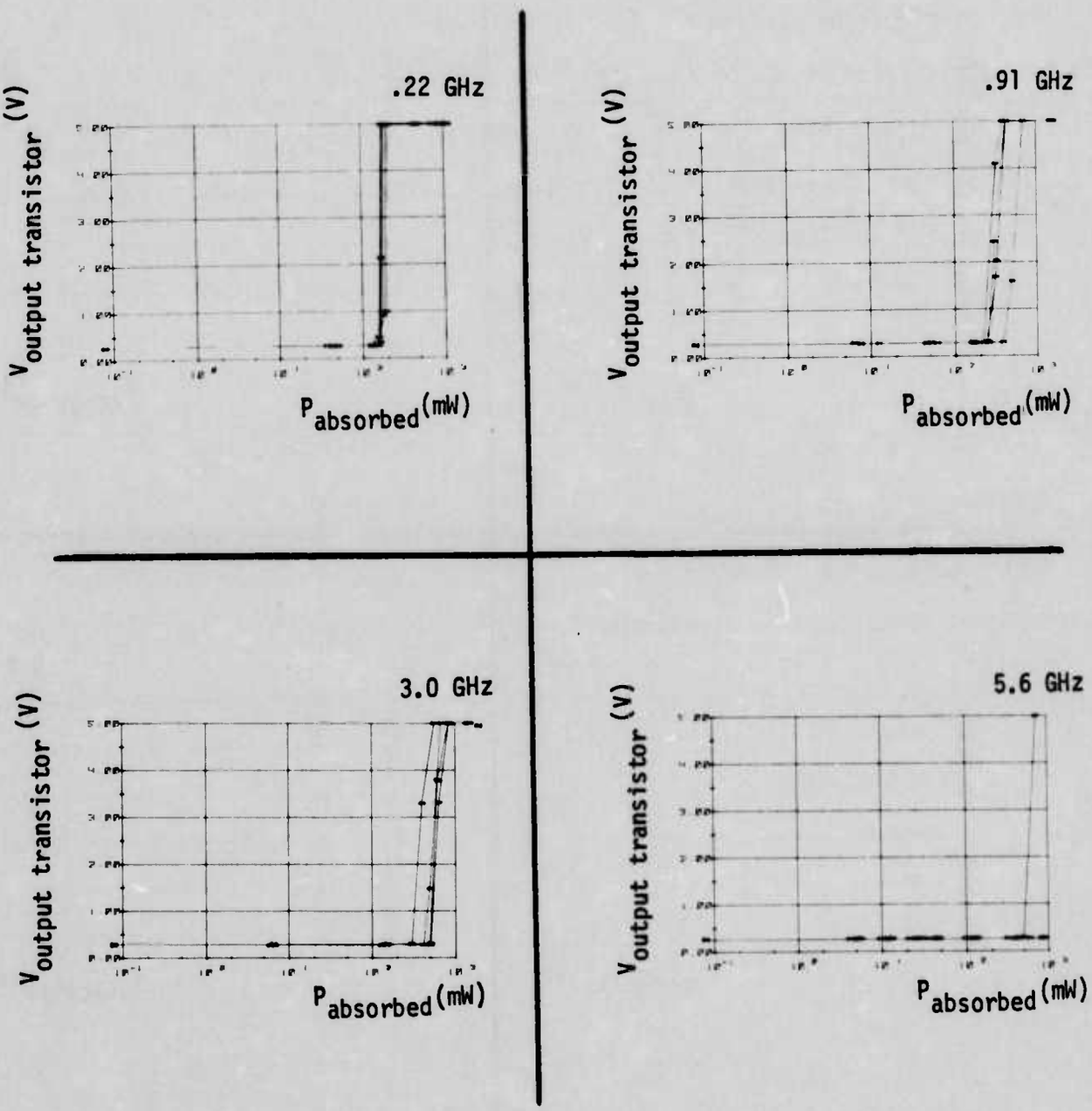


FIGURE 19 2002 INTERFERENCE DATA FOR RF INJECTED INTO THE NAND GATE INPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

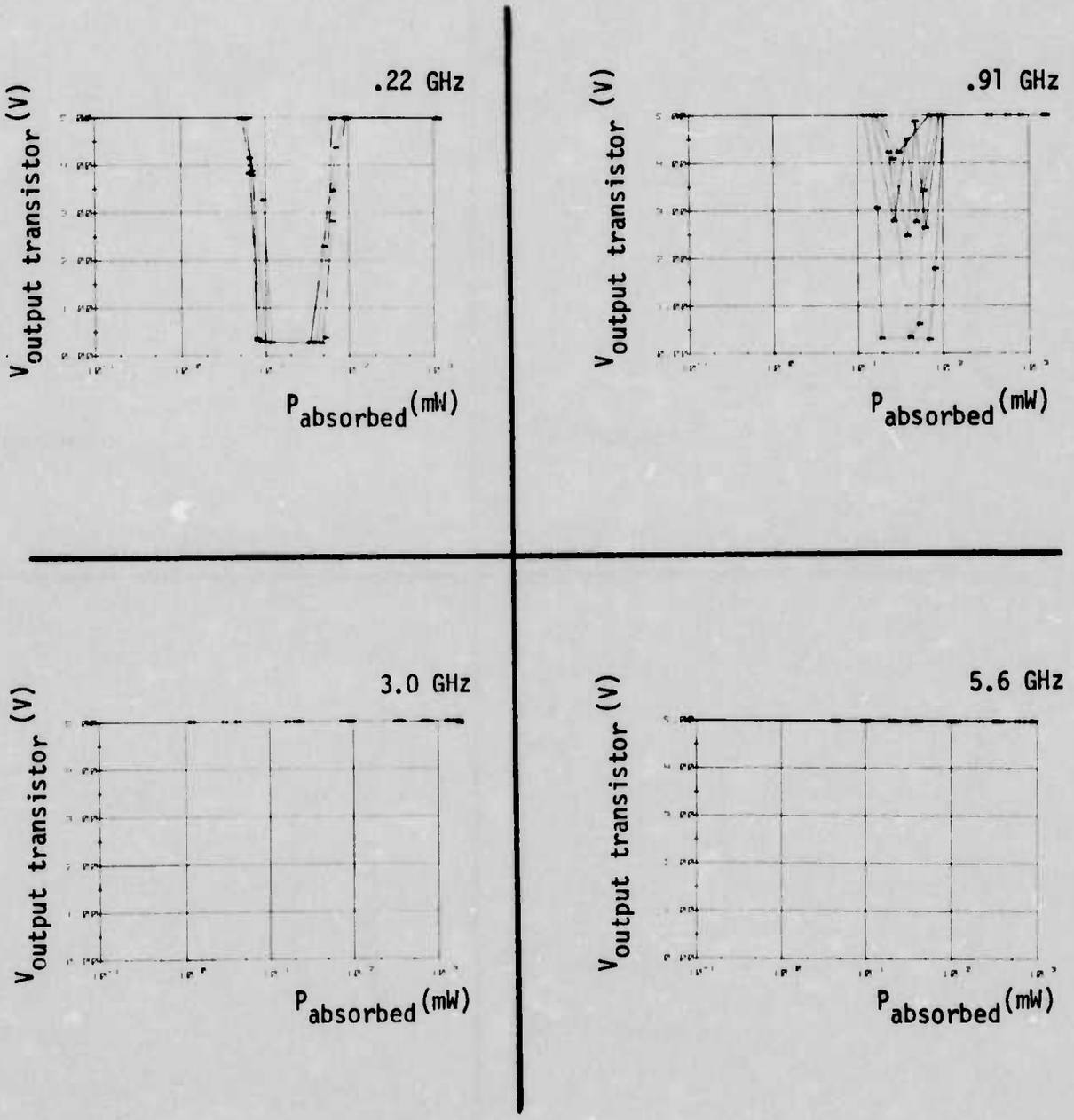


FIGURE 20 2002 INTERFERENCE DATA FOR RF INJECTED INTO THE NAND GATE INPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE LOW

3. RF CATASTROPHIC FAILURE TESTS

Catastrophic failure tests were performed on the 4011 and the 2002 at four interference frequencies for the most susceptible configurations. For similarity with the 7400 failure data, a Bruceton-type test was utilized for average failure level due to injection of a single 500 microsecond RF pulse. Ten devices were utilized for each susceptible configuration at each test frequency.

3.1 4011 Catastrophic Failure Tests - The two most susceptible 4011 circuit configurations were chosen for failure testing: RF injected into the input port with the output low and RF injected into the output port with the output low. Ten devices were used for each susceptible configuration: five devices from interference testing for the same susceptible configuration and five devices from interference testing for a similar non-susceptible configuration. With only ten devices, a Bruceton test can only give an approximate mean failure level. Additional devices were used for preliminary tests to determine the approximate mean and standard deviation of the failure level.

3.1.1 4011 Catastrophic Failure Test Circuit - The test circuit used for the 4011 catastrophic failure testing is shown in figure 21. All devices were operationally biased during actual failure testing. Special circuitry was utilized in some cases to determine if the device had actually failed.

3.1.2 4011 Catastrophic Failure Test Results - For all cases the output voltage was measured for both input bias state configurations before and after the injection of the single RF pulse. Figure 22 illustrates the mean failure levels for the two most susceptible configurations at each of the four frequencies.

All devices subjected to catastrophic failure testing were opened and surveyed for RF damage. Typical photomicrographs of the various types of RF damage are shown in figure 23 for the case of RF injected into the input port with the output

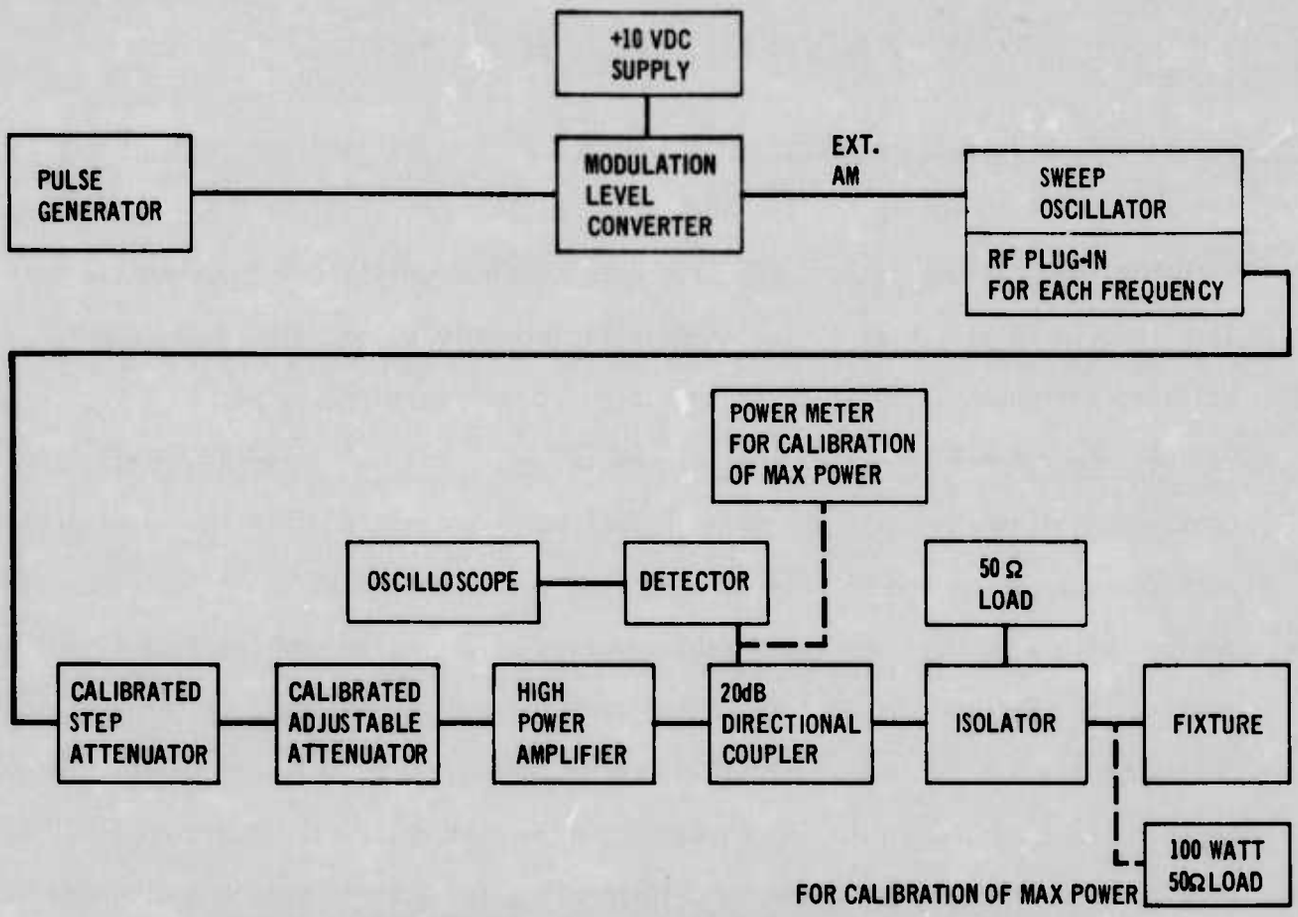


FIGURE 21 4011 CATASTROPHIC FAILURE GENERAL TEST SETUP

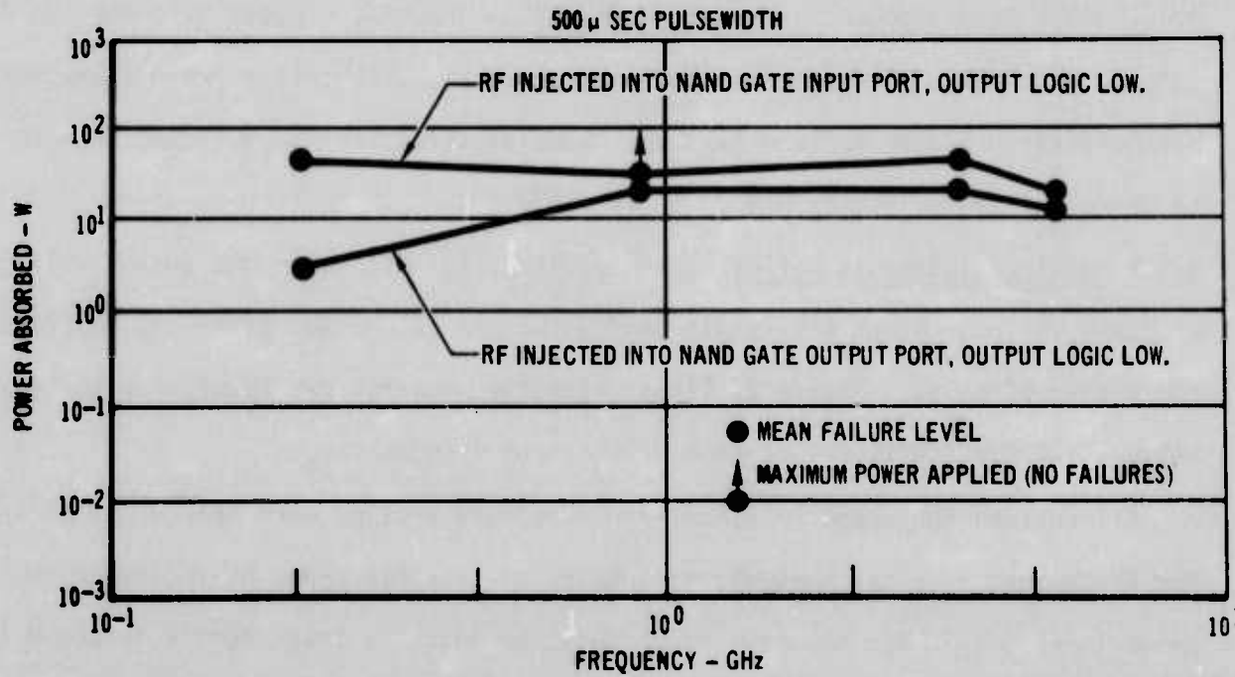
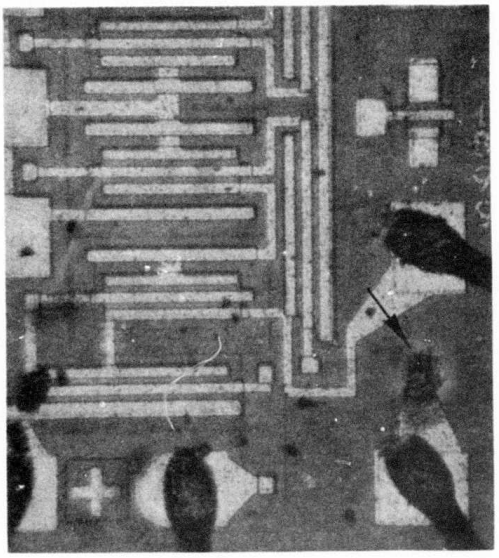
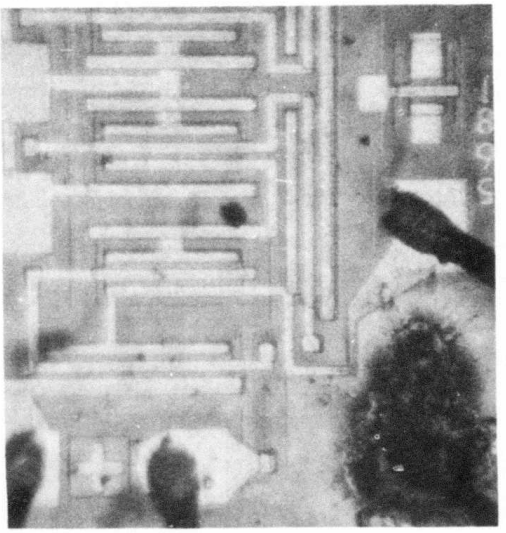


FIGURE 22 MEAN 4011 FAILURE LEVELS FOR MOST SUSCEPTIBLE CIRCUIT CONFIGURATIONS





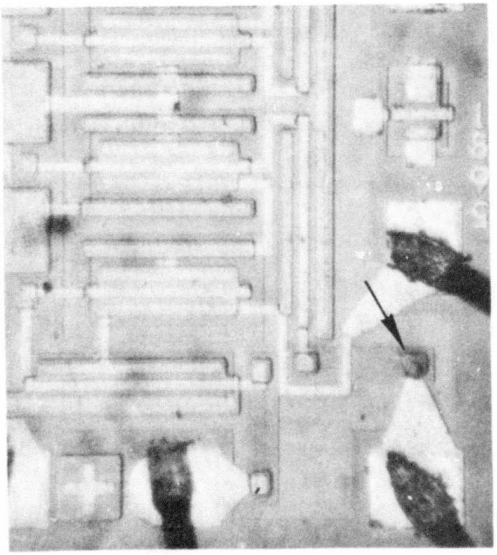


FIGURE 23 TYPICAL 4011 DAMAGE AREAS FOR RF INJECTED INTO THE INPUT PORT WITH THE OUTPUT LOW

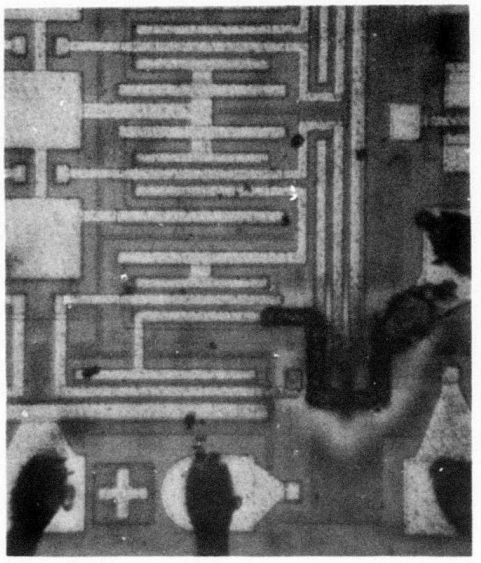
low. For the input RF injection case the damage areas of figure 23 correspond exceedingly well with the input protective diode which is postulated to be the source of the interference rectification [7]. In some cases the metallization is also blown in the vicinity of the RF injection port.

Figure 24 illustrates photomicrographs of typical RF damage areas for the case of RF injected into the output port with the output low. For the output RF injection case the damage areas of figure 24 are shown to be the metallization stripe up to the first output transistor. Evidently this metallization is the weakest link in the path of the injected RF and is destroyed before the RF can damage the transistor junctions which have been postulated as the source of the interference rectification for this case. There are no discrepancies between the possible rectification sites indicated by the interference data and the damage site found after catastrophic failure testing.

3.2 2002 Catastrophic Failure Tests - Two out of the three susceptible 2002 circuit configurations were chosen for failure testing: RF injected into the NAND gate output logic port (also output transistor base through resistor) with its output high and RF injected into the second NAND gate input with its output high. Ten devices were used for each failure test configuration: five devices from interference testing in the same susceptible configuration and five other devices from either a different test configuration or unused devices. A Bruceton-type test was performed on the ten samples as outlined previously for the 4011 devices.

3.2.1 2002 Catastrophic Failure Test Circuit - The RF test circuit used for 2002 catastrophic failure testing is identical to the 4011 failure test setup shown in figure 21. All devices were operationally biased during failure testing.

3.2.2 2002 Catastrophic Failure Test Results - For all cases the output transistor collector voltage was measured for both input bias states before and after the



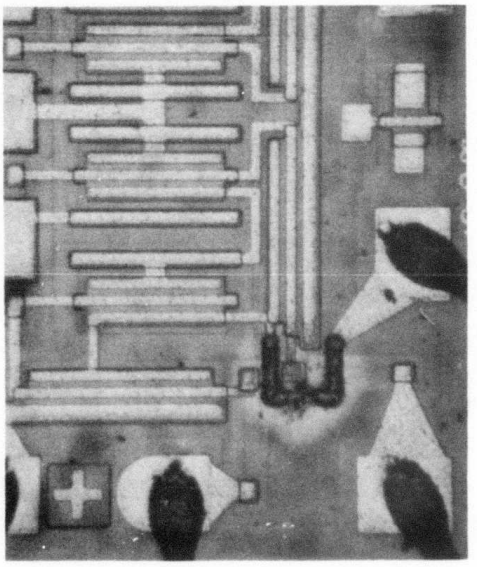


FIGURE 24 TYPICAL 4011 DAMAGE AREAS FOR RF INJECTED INTO THE OUTPUT PORT WITH THE OUTPUT LOW

injection of the RF pulse. The failure determination was made from these data. Figure 25 illustrates the mean failure levels for the two most susceptible configurations at each of the four frequencies.

All devices subjected to failure testing were opened and surveyed for RF damage. Typical photomicrographs of the various types of RF damage are shown in figure 26 for the case of RF injected into the input port with the NAND gate output logic high. The only damage area for this test configuration was the junction area and adjacent metallization on the input port diodes. Figure 27 illustrates photomicrographs of typical RF damage areas for the case of RF injected into the NAND gate output logic port with the output logic state high. The failure mechanism for this configuration is the collector-emitter metallization flow which shorts the logic output port to ground.

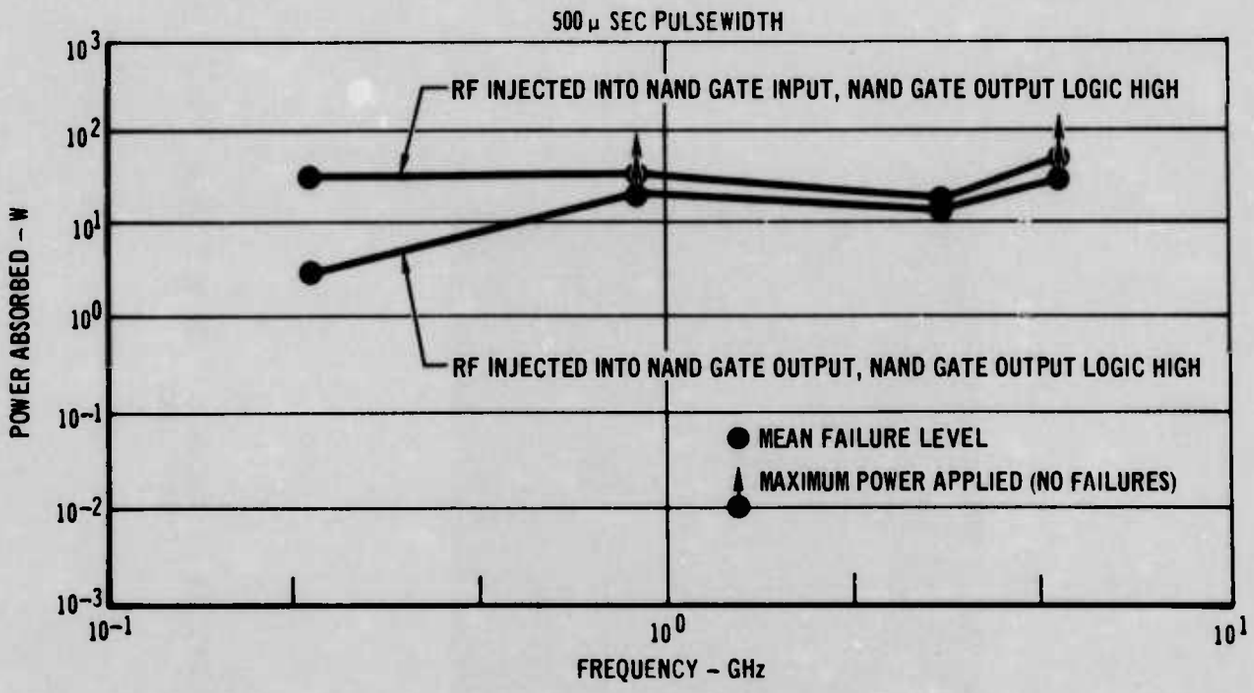
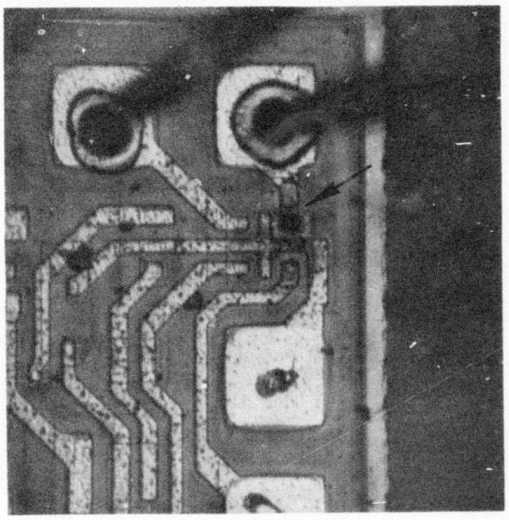
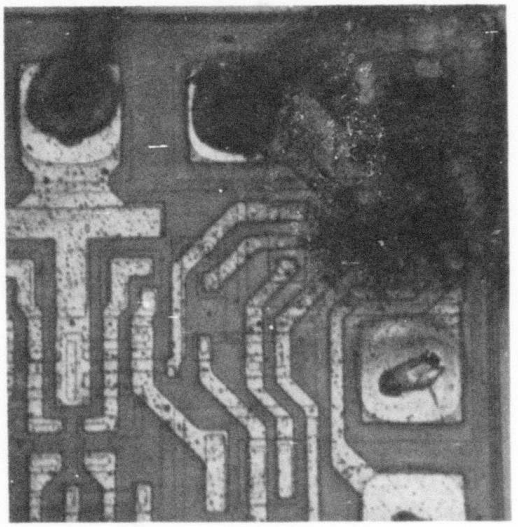


FIGURE 25 MEAN 2002 FAILURE LEVELS FOR TWO SUSCEPTIBLE CIRCUIT CONFIGURATIONS





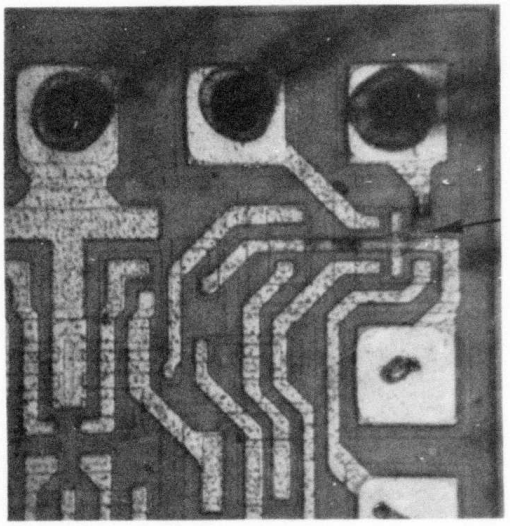


FIGURE 26 TYPICAL 2002 DAMAGE AREAS FOR RF INJECTED INTO THE NAND GATE INPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

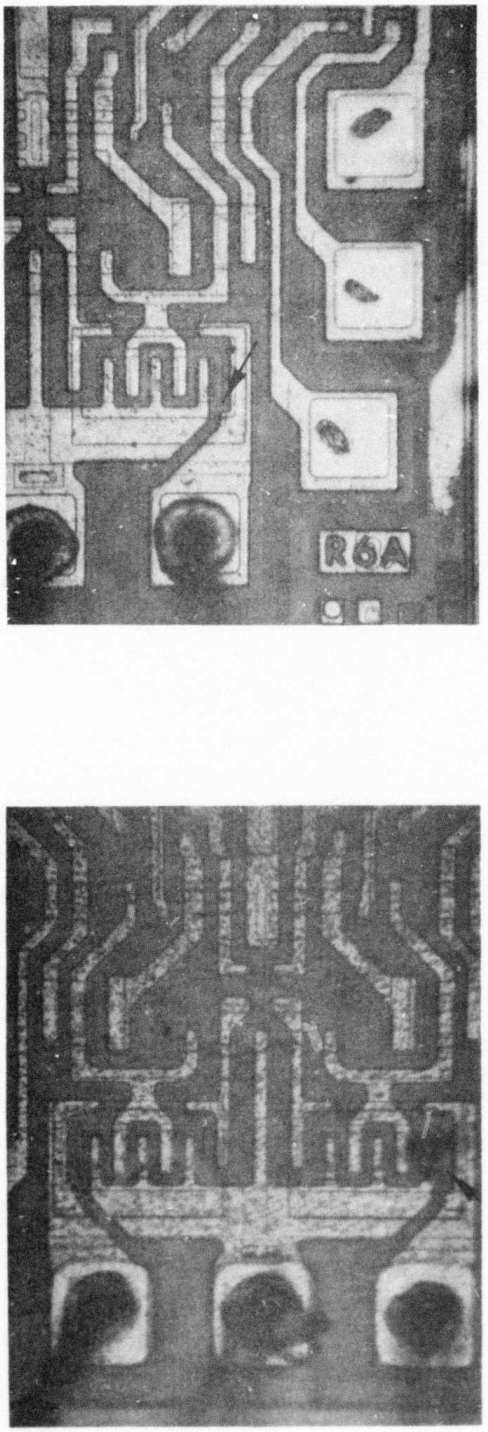


FIGURE 27 TYPICAL 2002 DAMAGE AREAS FOR RF INJECTED INTO THE NAND GATE OUTPUT LOGIC PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

4. BIPOLAR DATA COMPARISON

The purpose of this section is to determine if significant differences exist between the RF susceptibility characteristics of the 4011 CMOS and 2002 hybrid devices as related to the 7400 bipolar device.

4.1 4011/7400 Comparison - A direct CMOS-bipolar RF susceptibility comparison is given for functionally similar devices: the 4011 CMOS NAND gate and the 7400 TTL NAND gate.

4.1.1 4011/7400 Interference Test Comparison - Previous work [7] has indicated that the CMOS 4011 and the bipolar 7400 minimum RF susceptibility thresholds are very similar.

The most susceptible configuration for the 4011 is the output biased low with RF injected into the output port. This configuration is also the most susceptible one for the 7400. Data plots of the output voltage variations of the 4011 and the 7400 for various absorbed RF power levels are shown in figure 28. This comparison indicates that the 7400 is generally more susceptible than the 4011 by a factor of two, although a comparison of individual devices may be quite different. The calibration factor, which relates incident RF power to absorbed RF power, is slightly higher for the 7400 than for the 4011 for their most susceptible configuration. These data indicate that the 7400 is slightly more susceptible than the 4011 with respect to incident RF power.

The major interference mechanism for both types of devices is rectification and this can be explained by the bipolar pn junction rectification theory. The rectification mechanism is similar for both types of devices but the circuit reaction to these interference effects is different.

4.1.2 4011/7400 Catastrophic Failure Test Comparison - A comparison of failure levels for the 4011 and 7400 devices is shown in figure 29 for the case of RF

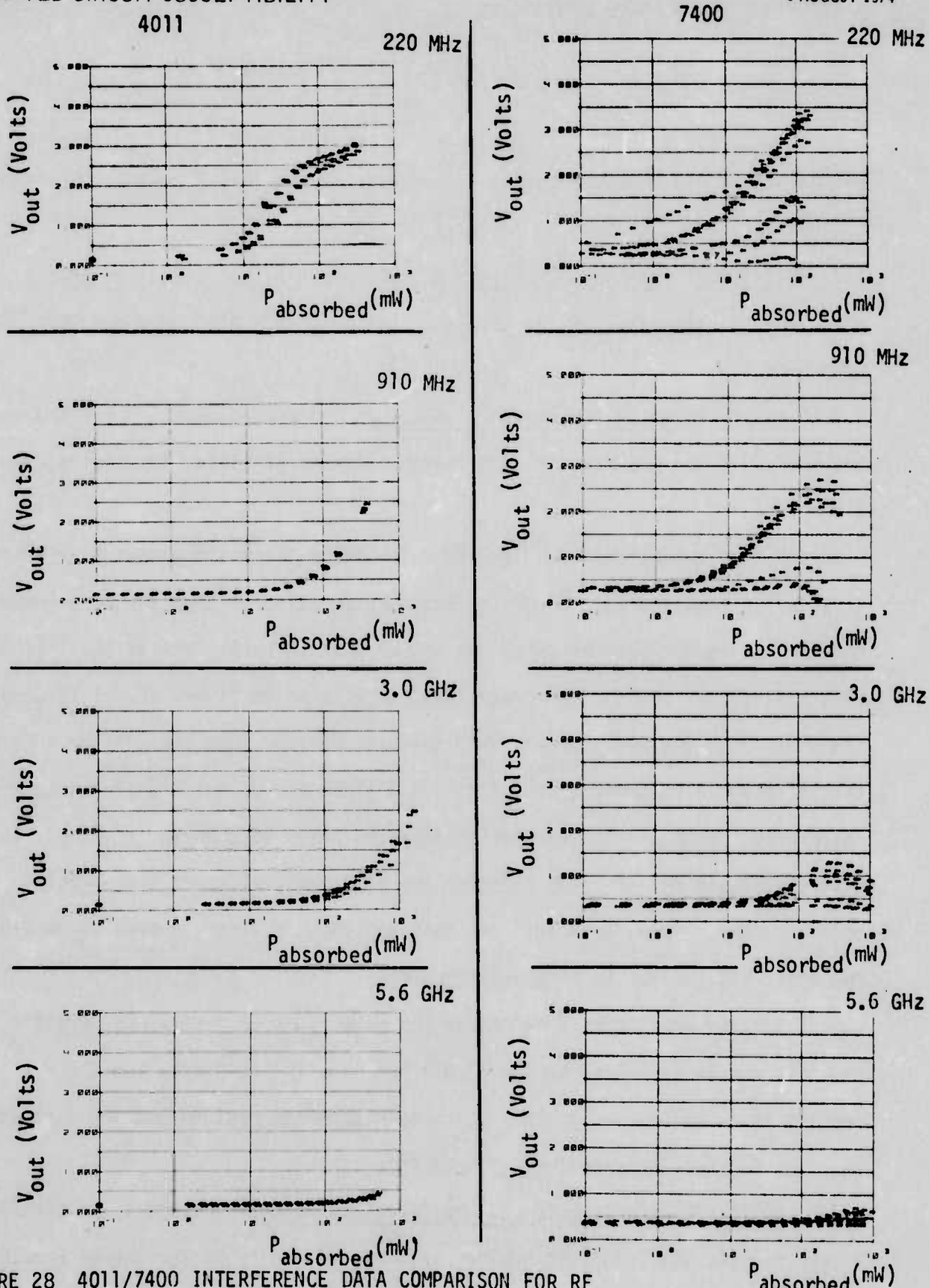


FIGURE 28 4011/7400 INTERFERENCE DATA COMPARISON FOR RF INJECTED INTO THE OUTPUT PORT, OUTPUT LOW

injected into the input port. As illustrated in figure 29, the 7400 is generally more susceptible to catastrophic failure for this configuration than the 4011.

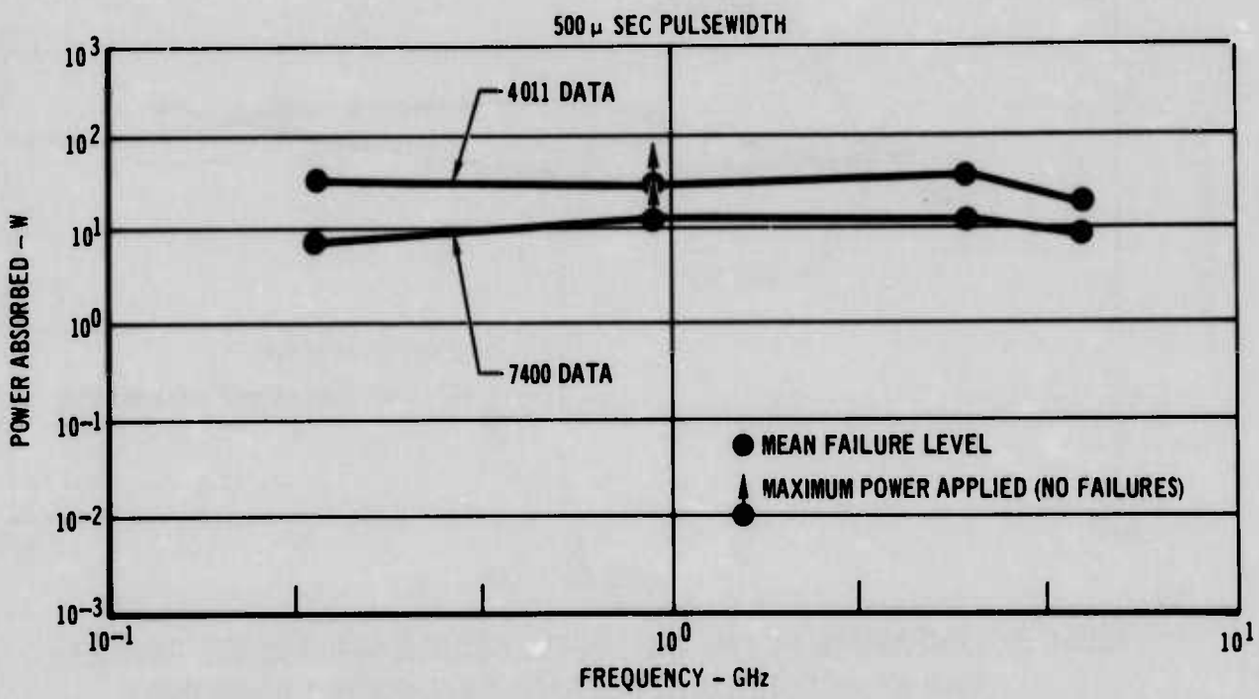


FIGURE 29 COMPARISON OF FAILURE LEVELS FOR THE 7400 AND 4011 DEVICES WITH RF INJECTED INTO THE NAND GATE INPUT PORT, OUTPUT LOGIC LOW

A comparison of failure levels for the 4011 and 7400 devices for the case of RF injected into the output port is shown in figure 30. This figure indicates that for this configuration the 4011 is more susceptible to catastrophic failure at some frequencies (220 MHz and 5.6 GHz) than the 7400. Of the two digital devices tested for catastrophic failure, the 4011 exhibits the lowest absorbed power injection level for failure ($\approx$3 Watts at 220 MHz). All failure modes for both types of devices were similar: bond wires, pn junctions and metallizations.

4.2 2002/7400 Comparison - An RF susceptibility comparison is presented between the 7400 bipolar NAND gate and the 2002 hybrid high power driver. Although minimal analysis has been done on the 2002 data, general comparisons are made for similar circuit configurations.

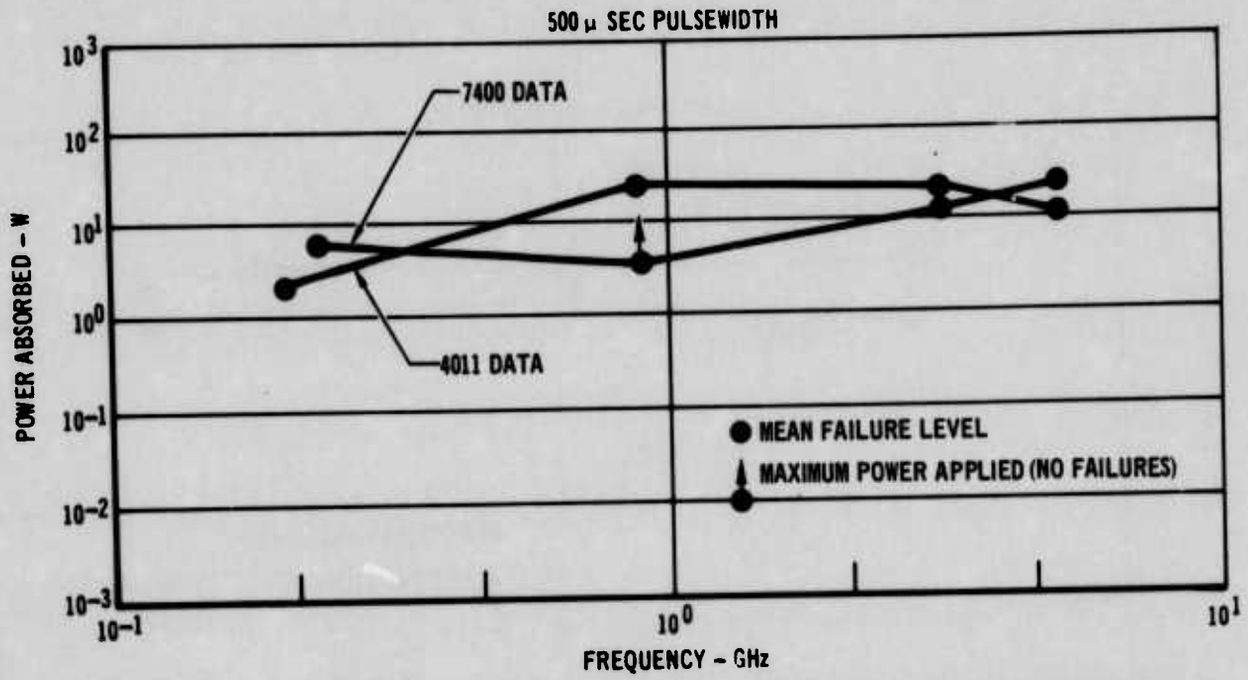


FIGURE 30 COMPARISON OF FAILURE LEVELS FOR THE 7400 AND 4011 DEVICES WITH RF INJECTED INTO THE NAND GATE OUTPUT LOGIC PORT, OUTPUT LOGIC LOW

4.2.1 2002/7400 Interference Test Comparison - Three separate 2002 circuit configurations were tested for RF interference as shown previously in figure 17. The 7400 TTL NAND gate logic configurations are compared with the DTL NAND gate logic configurations of the 2002 for circuit similarity.

Figure 31 compares the 7400 and 2002 for the configuration of the NAND gate output logic high with RF injected into the input port. For this configuration the 2002 is more susceptible than the 7400 although the difference is less than 6 dB. The susceptibility in each case decreases with increasing frequency.

For the configuration of the NAND gate logic output low with RF injected into the input port, the 7400 is not susceptible for absorbed power levels up to 1 watt. The 2002, however, is susceptible for this configuration as shown in figure 20 and the susceptibility decreases with increasing frequency.

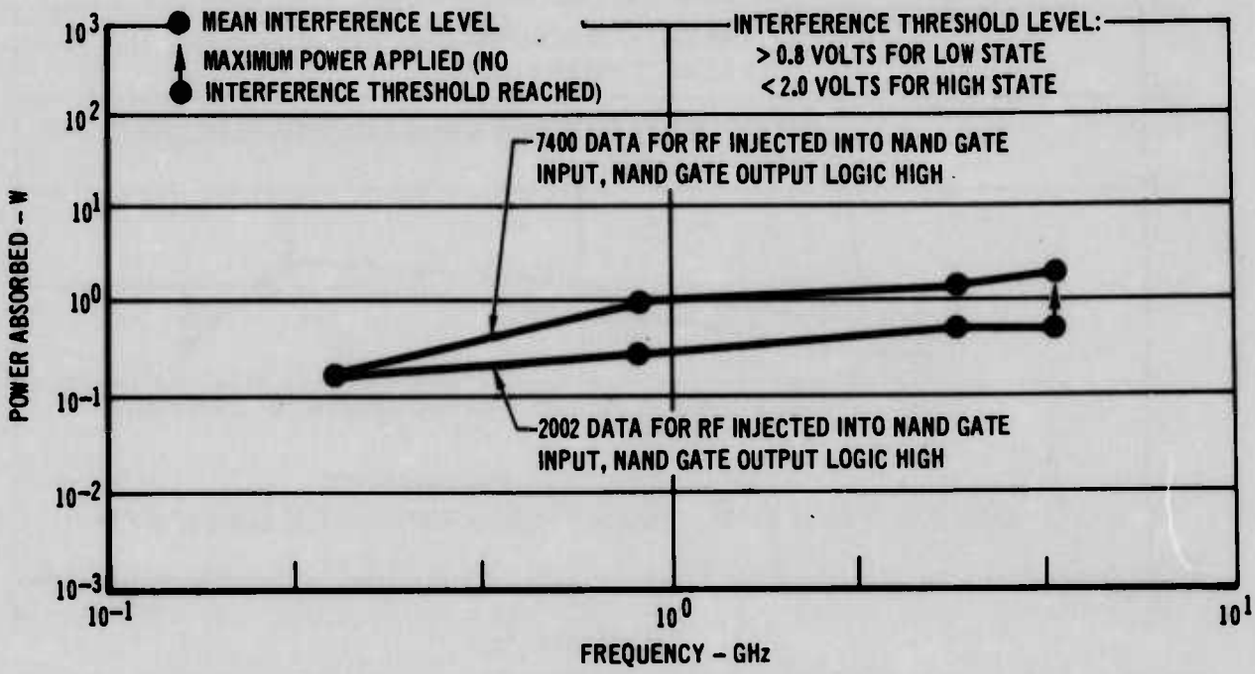


FIGURE 31 COMPARISON OF INTERFERENCE THRESHOLD LEVELS FOR THE 7400 AND 2002 DEVICES FOR RF INJECTED INTO THE NAND GATE INPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

Figure 32 compares the 7400 and 2002 for the configuration of the NAND gate output logic high with RF injected into the output logic port. The 7400 data for this configuration is somewhat erratic with susceptibility present only for some devices at 3.0 GHz. The 2002 data indicates an erratic low frequency susceptibility with only two devices exhibiting output logic state transitions at 220 MHz.

The 2002 was found to be unsusceptible in preliminary tests for the configuration of RF injected into the NAND gate output port with the NAND gate output logic state low. The 7400 was found to be susceptible for this configuration at the three lowest frequencies (.22, .91, and 3.0 GHz).

The predominant mechanism for RF effects in the 2002 and 7400 is thought to be rectification of RF at the device pn junctions although the circuit reaction to these effects may vary as can be seen.

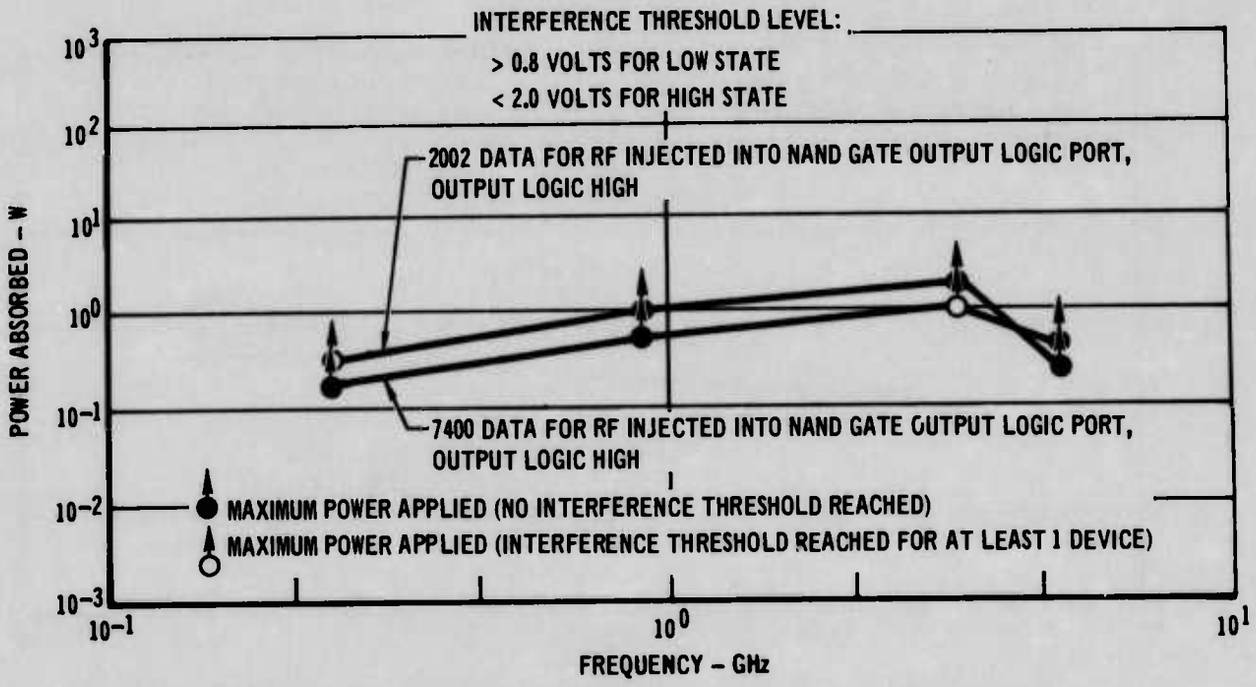


FIGURE 32 COMPARISON OF INTERFERENCE THRESHOLD LEVELS FOR THE 7400 AND 2002 DEVICES FOR RF INJECTED INTO THE NAND GATE OUTPUT LOGIC PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

4.2.2 2002/7400 Catastrophic Failure Test Comparison - A comparison of failure levels for the 2002 and 7400 devices is shown in figure 33 for the case of RF injected into the NAND gate input port with the NAND gate output logic state high. The 2002 is shown to be less susceptible to catastrophic failure than the 7400 for this configuration, in most cases by as much as 6 dB.

A comparison of failure levels for the 2002 and 7400 devices is shown in figure 34 for the case of RF injected into the NAND gate output port with the NAND gate output logic state high. Again the 2002 is shown to be generally less susceptible to catastrophic failure than the 7400 for this configuration.

All failure modes for both types of devices were similar: bond wires, pn junctions and metallizations.

4.3 4011/2002/7400 Comparison - The CMOS 4011, the hybrid 2002 and the bipolar 7400 devices are compared for relative susceptibility to RF power. Individual

device and circuit comparisons can be insignificant because of the different circuit effects produced by the injected RF. For this reason the minimum power level required for a device susceptibility level to be exceed was chosen as the comparison measure. This comparison is made for the most susceptible device configuration at a given frequency.

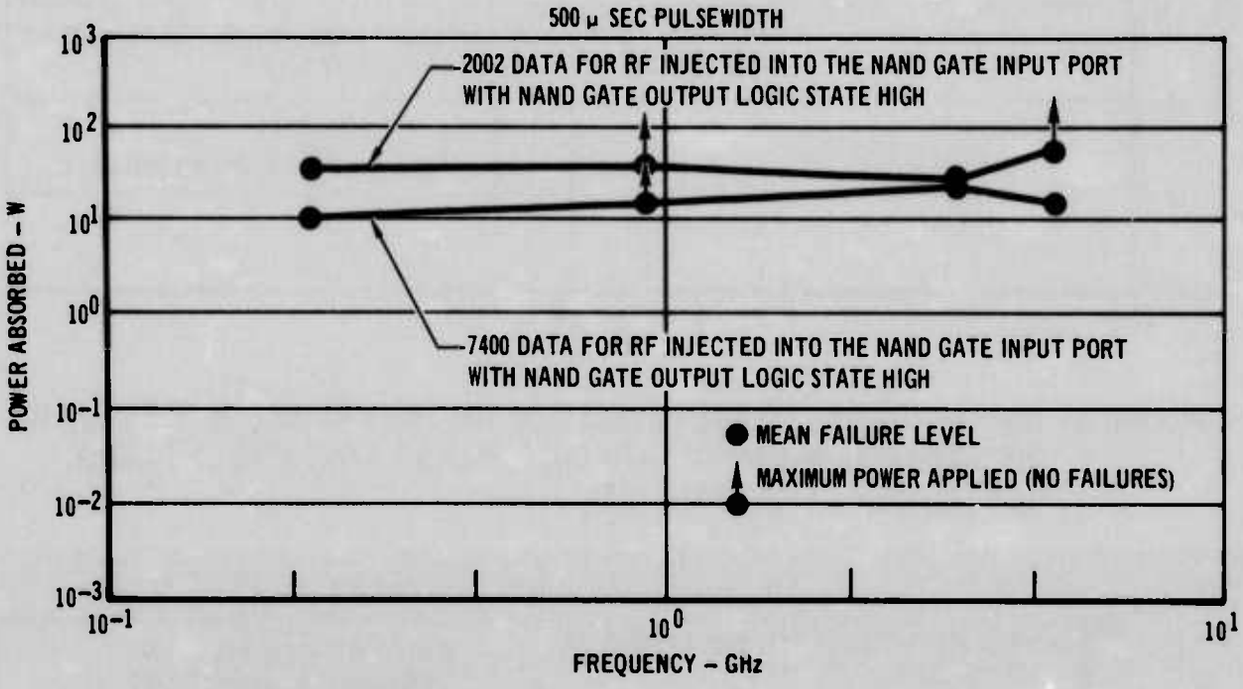


FIGURE 33 COMPARISON OF FAILURE LEVELS FOR THE 7400 AND 2002 DEVICES FOR RF INJECTED INTO THE NAND GATE INPUT PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

A device comparison for minimum interference threshold level at the four test frequencies is shown in figure 35. The interference levels are chosen from the individual device specification sheets. As shown in figure 35, the variation from device to device (technology to technology) at a given frequency is approximately 10 dB. At 5.6 GHz, the interference level was not reached at the maximum power level of the automated test system for the 4011 and 2002 devices. For their most susceptible configurations, the most susceptible CMOS devices are less susceptible than the most susceptible bipolar and hybrid devices.

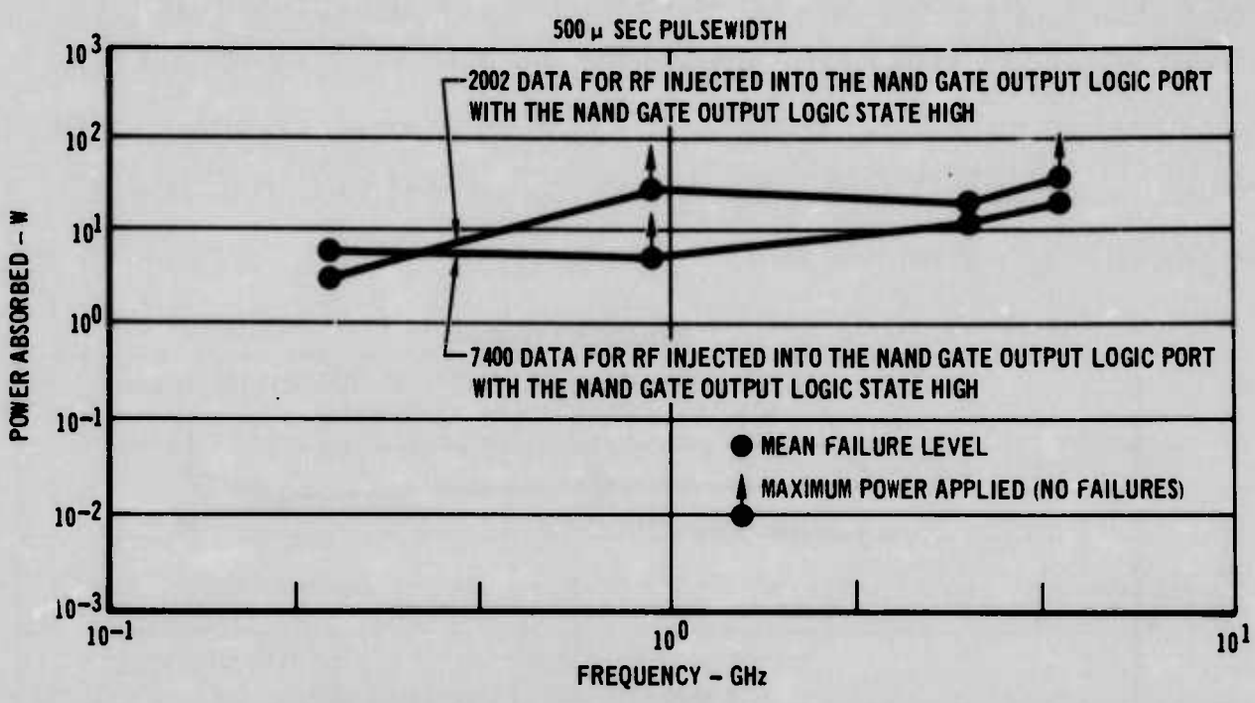


FIGURE 34 COMPARISON OF FAILURE LEVELS FOR THE 7400 AND 2002 DEVICES FOR RF INJECTED INTO THE NAND GATE OUTPUT LOGIC PORT WITH THE NAND GATE OUTPUT LOGIC STATE HIGH

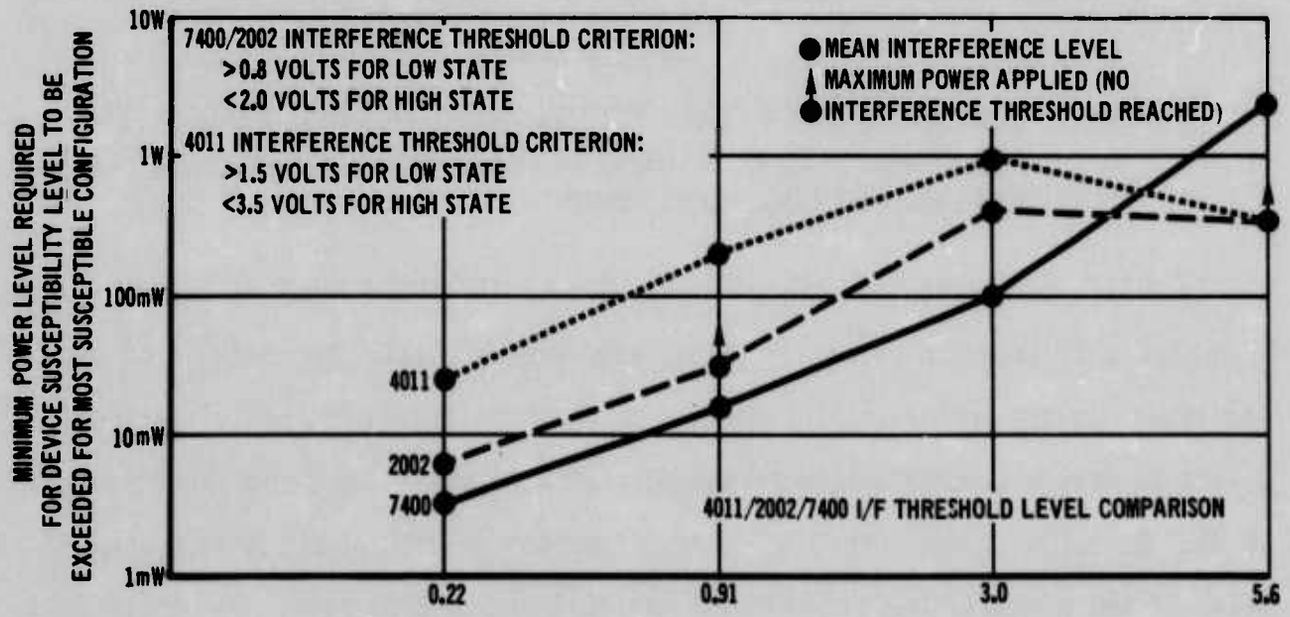


FIGURE 35 4011/2002/7400 MINIMUM INTERFERENCE LEVEL COMPARISONS AT FOUR FREQUENCIES

The catastrophic failure comparisons for all three devices at four frequencies is shown in figure 36. This comparison is for the minimum peak power level to cause failure for the most susceptible test configuration. Again the minimum failure levels for all three types of devices at all four test frequencies are within a 10 dB band. The power level band for failure falls approximately 30 dB higher than the power level band for minimum interference threshold level. All failures observed in all devices fall in three categories: melted bond wires, pn junction failure and metallization vaporization.

For the three devices tested, it appears that significant improvements in RF susceptibility can not be realized by using devices fabricated by a preferred technology.

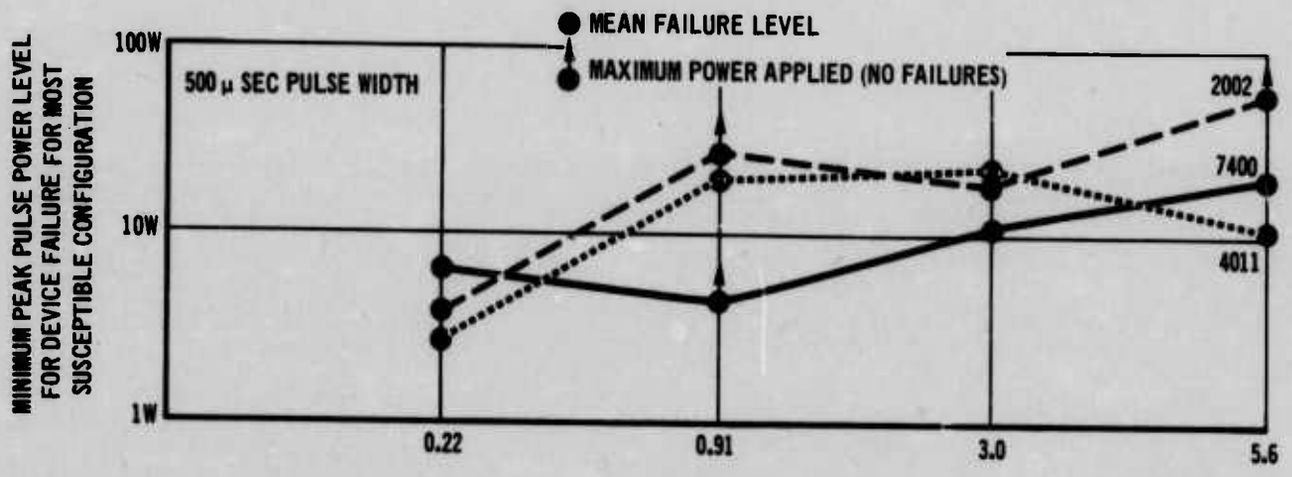


FIGURE 36 4011/2002/7400 FAILURE LEVEL COMPARISON AT FOUR FREQUENCIES

5. CONCLUSIONS

The RF susceptibility in the MOS and hybrid devices tested (4011 and 2002) can be explained using the same mechanism as in the bipolar 7400: rectification in the pn junctions. Preliminary analysis on the RF effects in the MOS 4011 indicate that rectification is occurring at the protective and parasitic junctions and the circuit is reacting normally to the RF generated DC currents. More work is required to completely characterize these junctions and to compare their efficiency, frequency response, etc., with bipolar junctions. This should lead to a general rectification theory which can be used for both bipolar and MOS devices.

Very little analysis has been done on the hybrid 2002 device but all RF effects are generally consistent with the rectification theory developed for the bipolar 7400. Additional work is required to determine the characteristics of their RF induced current generators and to analyze the circuit response to these currents. This characterization and analysis should lead to a general rectification model applicable to all semiconductor devices containing pn junctions.

The mean power level required for the output voltage to cross the interference threshold level for the 7400, 4011 and 2002 devices falls within a 10 dB band at all four frequencies for the most susceptible port. The minimum power level required for catastrophic failure for all three types of devices also falls within a 10 dB band which is generally 30 dB above the minimum interference threshold level band.

Thus, it appears that fabrication technology, per se, is not a significant factor in the RF susceptibility characteristics of semiconductor devices in general.

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